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Gallium nitride powerbar transistors with via holes fabricated by laser ablation

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Low ohmic through-hole vias are fabricated for AlGaN/GaN HEMT powerbar devices on SiC substrates using laser ablation technique. A complete processing technique has been developed. Through-wafer micro holes with an aspect ratio of 4 were drilled using pulsed UV laser machining. A plating technique on steep side wall could be established. Feasibility and performance of laser drilled via holes were tested with large power devices and proved successful up to the packaging level. The device demonstrated 14 dB of linear gain and a saturated output power of 40 W.

1 Introduction

The application of UV pulsed laser processing is a new approach to create via holes in 400 µm thick semi-insulating SiC wafers serving as substrate for AlGaN/GaN HEMTs. SiC is one of the hardest materials and is chemically inert. In order to take advantage of the superior heat sinking and heat spreading properties of SI-SiC for microwave L-band power transistors it is advantageous to use the full wafer thickness instead of thinning down. Due to its extreme properties, dry etching of SiC is limited by etch rate and aspect ratio of the desired holes.

The feasibility of laser-assisted fabrication of through-wafer via holes for AlGaN/GaN HEMTs on SiC has been proven. The complete process flow from CAD wafer layout to laser processing and metallization has been established. For reliable laser processing a high beam positioning accuracy of ±1 µm with respect to the device pattern on the wafer could be verified. The direct laser drilling approach offers a highly flexible way to create via holes without time-consuming wafer thinning, lithography and dry etching. Holes with smooth sidewalls can be drilled in SiC using an UV diode-pumped solid-state laser.

After completion of the front-end process micro holes are drilled from the back through ~400 µm thick semi-insulating silicon carbide wafers having AlGaN/GaN transistors on the front side [1–3]. The holes are conical with diameters of ~120 µm on the laser entrance and ~80 µm on the laser exit side. Following, an electrical connection between the backside and the front is realized by metallization of the sidewalls of the holes. The gold layer is completely closed and has a thickness of ~5 µm. The plated gold thickness is uniform for the vias with aspect ratios as high as ~4.

2 Processing

The pulsed laser beam is used to directly drill one hole at a time. The frequency-tripled, diode pumped solid state laser provides an output wavelength of 355 nm with a Gauss-shaped intensity profile [4]. The

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laser is focused to a spot size of ~15 µm in diameter. Typical pulse energies of 65 µJ/pulse at a laser pulse repetition rate of 20 kHz are used to create through-wafer micro holes. The desired hole diameter of ~100 µm is obtained by circular motion of the laser beam on the wafer. The micro holes are drilled from the backside of the wafer. For mechanical protection the front side of the wafer is covered by photo resist during processing.

The process of laser drilling is guided by CAD layout data. Drilling positions are designed altogether with the front-end layout in separate layers. Data for laser drilling are then converted to CNC compatible format. The laser processing starts with alignment using a vision system and automated pattern recognition. The laser workstation achieves an alignment precision of the center of the laser spot of ±1 µm with respect to existing structures. This accuracy can also be achieved when the alignment marks are placed on the side opposite to the one processed by the laser (front-to-backside alignment).

During laser processing the wafer stage is moved to the desired drilling position underneath the focusing optics and then the laser is switched on. The laser beam itself is moved by a galvo scanner during the drilling process. The holes are drilled from the backside through the wafer and the plated metallization pads on the front side. After laser drilling the inner surface of the hole is covered by a thin layer of re-solidified material from ablation. This material consists mainly of SiO_x and is easily removed by wet etching [5].

The electrical connection through the via hole is provided by evaporation of a plating base and subsequent electro plating. Proper alignment of the wafer in the evaporation apparatus is mandatory in order to achieve full metal coverage of the hole during plating base evaporation. On the front side of the wafer the photoresist is open on positions of the connecting pads. During plating the backside of the wafer and parts of the front that are opened up in the photoresist are in contact with the electrolyte. Therefore, the gold layer grows not only on the backside and on the sidewalls of the holes but also on the open area of the front side metallisation.

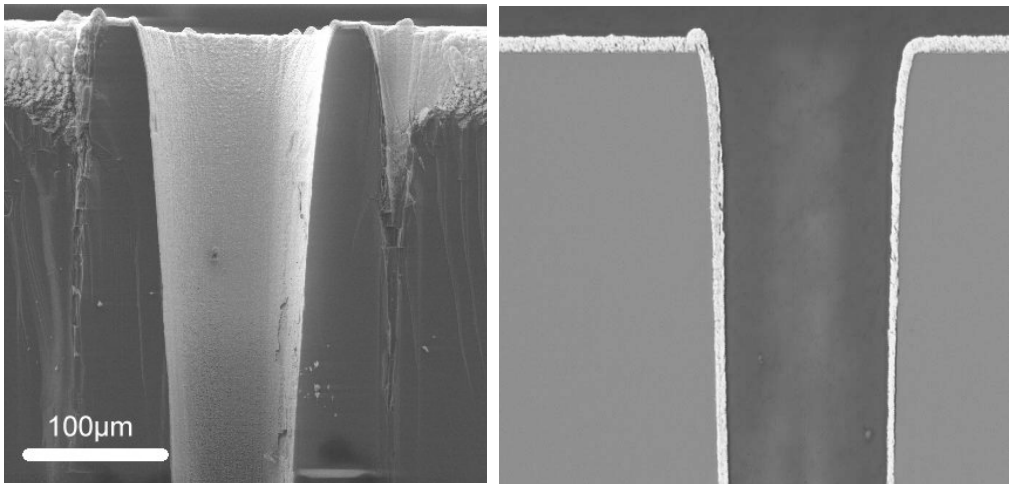

Fig. 1 Process steps of the via-hole fabrication. **Left:** On the left the cleaved SiC-wafer after laser drilling is shown. On the top left and right of the via-hole laser marks required for cleaving can be seen. **Right:** A via hole after completion of the via fabrication is presented. The plating layer covering the surface of the via-hole and extending to the backside of the wafer (on top) can be clearly distinguished from the SiC-wafer material. The thickness of the gold plating is around 5 µm.

3 Results

Additional experiments prove that a repeatable via process for electrical connection is obtained. For this purpose several test samples were prepared with an array of vias for resistance measurements. The resistance maps show good homogeneity and reproducibility of via-hole processing. Results from resistance

measurements from a set of 200 via holes are presented in Fig. 2 revealing that all vias are intact and the access resistance is quite similar for all devices under test.

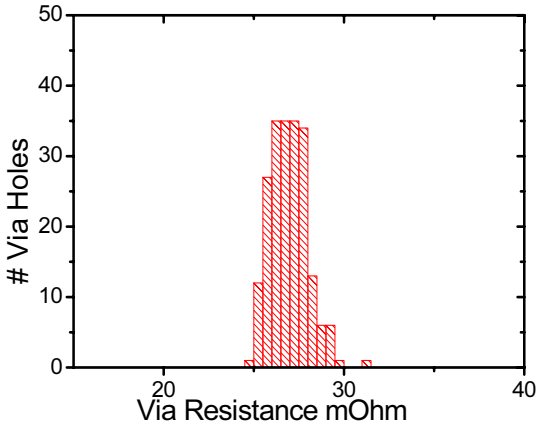

Fig. 2 Resistance measurements of through-hole vias.

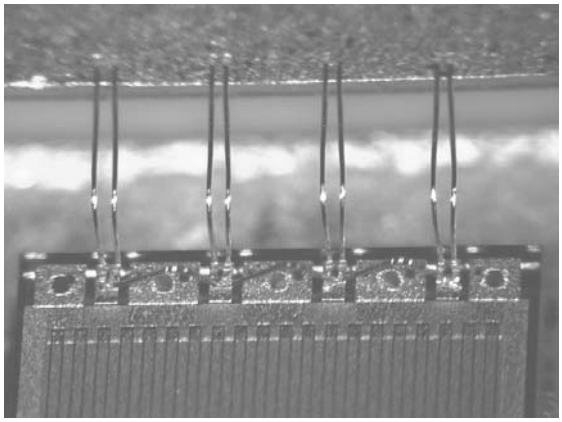

Fig. 3 AlGaN/GaN HEMT device (4x10x500 µm^3 L-band power bar) with laser drilled through-wafer vias mounted in power package (Close-up view).

AlGaN/GaN-HEMTs were processed on several wafers by the aid of via hole laser drilling. After completion of the front-end processing HEMT devices were characterized by DC and RF on-wafer measurements. Wafer maps of the transistor device characteristics and parameters were compared with those measured after laser backend processing. RF-load-pull measurements revealed no signs of degradation for the transistors after laser processing.

After dicing of the wafer the transistor devices were mounted in microwave packages and characterized by RF measurements. In Fig. 3 a high-power transistor having powerbar design is mounted. The chip with through-wafer vias is soldered onto the power package using Au/Sn preforms.

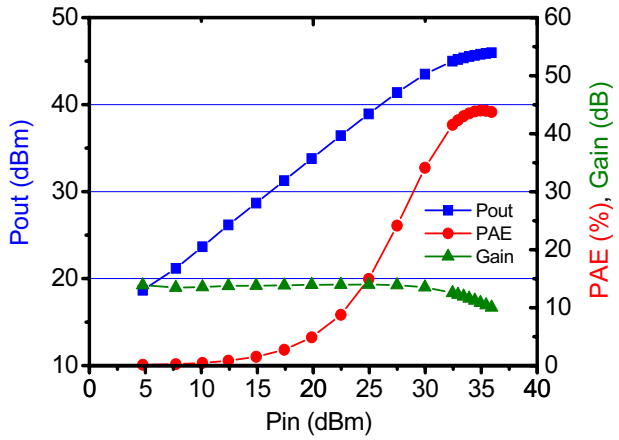

Fig. 4 Output power of an AlGaN/GaN HEMT with through-wafer vias operated at 2 GHz. The device having a total gate width of 18 mm was biased at 20 V and 2.3 A. A saturated output power of 40 W with an associated power added efficiency (PAE) of 43% was achieved.

Comparative examinations before and after laser drilling showed no change or degradation of transistor DC and RF properties due to laser processing. RF power measurements of AlGaN/GaN HEMTs using a power bar design and mounted with laser via technology revealed that this technique is operational and high power levels were achieved. As an example a powerbar having 9 subcells each containing 8 transistor fingers of 250 µm gatewidth is presented. This 9x8x250 μm^3 wide device was operated at a drain-source bias of V_{ds} = 20 V and a quiescent current of I_{dq} = 2.3 A. The device demonstrated 14 dB of linear gain and a saturated output power of 40 W. An associated power added efficiency (PAE) of 43 % was achieved.

4 Conclusion

Laser assisted via fabrication on 400 µm thick semi-insulating SiC was successfully demonstrated. Vias with an aspect ratio ~4 were used for the implementation in transistors having power bar design. The packaged AlGaN/GaN-HEMTs achieve a saturated output power of 40 Watt and an associated PAE of 43% at 2 GHz. In conclusion, the compatibility of laser processing of via holes with semiconductor device fabrication has been demonstrated. Laser micro ablation has been successfully tested as a promising alternative to plasma processing of hard and inert materials.

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