A Highly Survivable 3–7 GHz GaN Low-Noise Amplifier

Matthias Rudolph[1], Reza Behtash[1], Klaus Hirche[2], Joachim Würfl[1],
Wolfgang Heinrich[1], Günther Tränkle[1]
[1]Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH)
Gustav-Kirchhoff-Str. 4, D-12489 Berlin, Germany, (e-mail: rudolph@fbh-berlin.de)
[2]Tesat-Spacecom GmbH & Co. KG,
Gerberstr. 49, D-71522 Backnang, Germany

Abstract— **A highly rugged low-noise GaN MMIC amplifier is presented that operates in the frequency band 3–7 GHz. A noise figure *NF* below 2.3 dB is measured from 3.5 to 7 GHz, with *NF* < 1.8 dB between 5 and 7 GHz. The survivability of the LNA was assessed by several stress-tests, injecting in the input up to 36 dBm at 4 GHz for 16 hours. To the authors knowledge, these are the most severe survivability tests for these circuits reported in the literature so far.**

Keywords— **Amplifier noise, Integrated circuit noise, Microwave FET amplifiers, MMIC amplifiers, Noise, Semiconductor device noise**

I. Introduction

GaN HEMTs are excellent candidates for high-power, broadband, and highly efficient applications in the microwave and millimeter wave range. However, the power handling capabilities also can be beneficial in case of low-noise amplifiers (LNAs). One application are extremely linear low-noise amplifiers. Extracted third-order output intermodulation points as high as 38 dBm [1] and 43 dBm [2] have been reported. On the other hand, highly rugged LNAs that survive high levels of overdrive input power for a certain time are also desirable for receiver front-ends for various applications. While GaAs-based LNAs typically require the RF input power not to exceed approximately 20 dBm, it was reported that GaN-based LNAs survived measurement up to 23 dBm [3], 30 dBm [2], almost 31 dBm [4], and 36 dBm cw and 46 dBm pulsed power [5]. These LNAs offer interesting possibilities for simplified receiver front-end concepts, since, e.g., an input protection circuit can be omitted that is required when using conventional technology.

In this paper, we present a highly survivable 3–7 GHz GaN-based LNA. Its electrical and noise performance are competitive with the results presented in the literature [1–6]. However, the main focus lies on the survivability assessment of the circuits. Not much data has been disclosed on this issue so far. In the case of [2] and [3], the power performance of the LNA was repeatedly measured sweeping the input power up to a certain value (30 dBm and 23 dBm, respectively), without damaging the device in a way that is visible in the power measurement. In [4], the input power was increased until destruction of the LNA at 31 dBm. In [5], 36 dBm of cw power and 46 dBm of pulsed power with 10% duty cycle were applied for 1 min without causing visible changes in the post-stress LNA gain. In this work, on the other hand, high input powers are injected into the LNA which is biased for low-noise operation. Several frequencies (2 GHz–5 GHz), power levels (20 dBm–36 dBm), and measurement times (10 min–16 h) were tested at altogether nine LNAs. To the best of the authors' knowledge, these measurements exceed the cw stress conditions presented in the literature significantly.

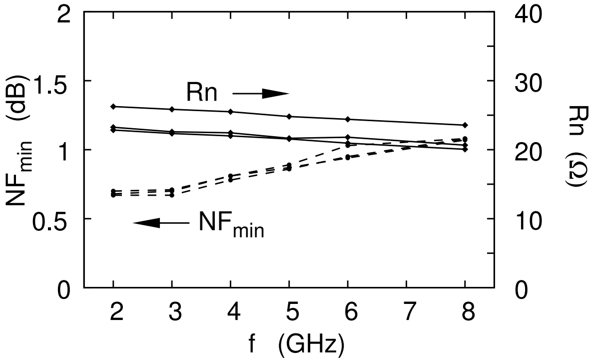


Fig. 1. Noise figure *NF* and equivalent noise resistance R_n of 4×50µm FET at low-noise bias condition $V_{ds} = 8$ V, $I_{ds} = 10$, 20, and 30 mA.

II. GaN FET Technology

In this work the AlGaN/GaN heterostructure is grown on a 2″ S.I. SiC substrate by metal-organic vapor phase epitaxy. The layer structure is as follows: a 2.3 µm GaN buffer layer, a 3 nm $Al_{0.3}Ga_{0.7}N$ spacer layer, a 12 nm 5×10^{18} cm^{-3} Si-doped $Al_{0.3}Ga_{0.7}N$ supply layer, a 10 nm $Al_{0.3}Ga_{0.7}N$ barrier layer and a 5 nm GaN cap layer. An averaged sheet resistance of 375 Ω/□ was measured using Van-der-Pauw structures on the passivated wafer.

The MMICs were realized through a 2″ stepper technology at the FBH with the following process steps: After the lithography of the Ohm-level Ti/Al/Ti/Au was evaporated and capped with a sputtered layer of WSiN as ohmic metalization. Annealing of the contacts at 830°C results in an ohmic contact resistance of 0.4 Ωmm. The mesa structures

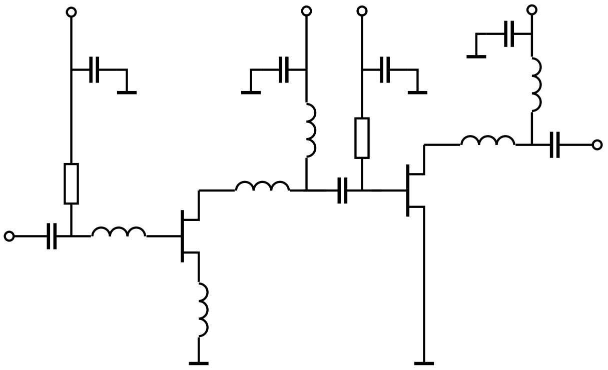


Fig. 2. Circuit schematic of LNA.

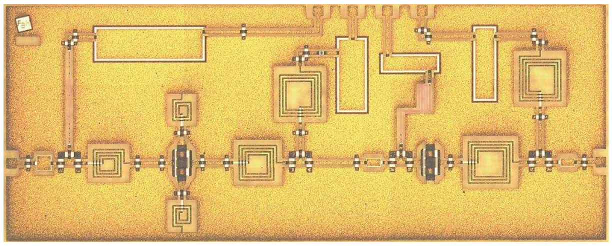


Fig. 3. Chip photo of fabricated two-stage LNA.

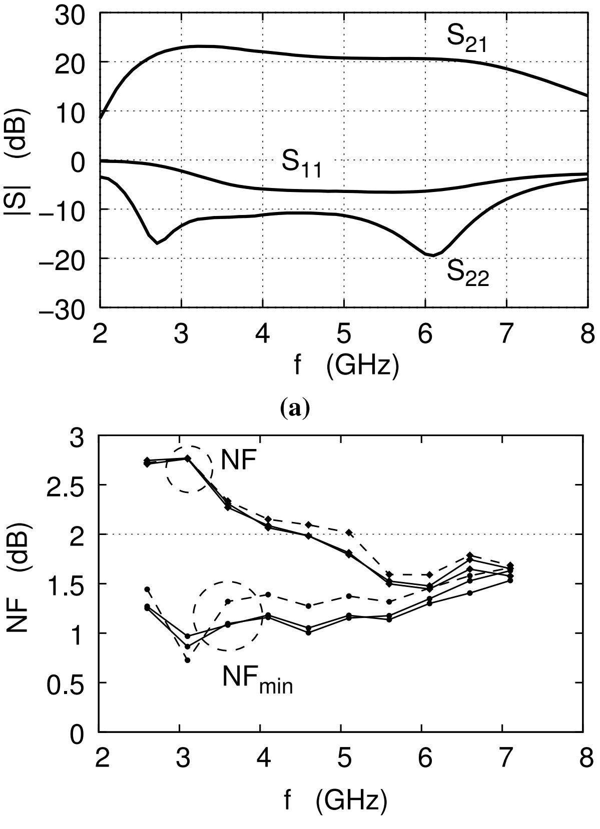
were realized by reactive ion etching using a Ar/BCl_3/Cl_2 plasma. 0.4 µm electron-beam defined Pt/Au contacts were used as Schottky T-gates. Si_3N_4 MIM capacitors and NiCr resistors complete the coplanar MMIC process.

The noise performance of a 4×50 µm HEMT is shown in Fig. 1. The device is biased for low-noise operation at $V_{ds} = 8$ V, $I_{ds} = 10$, 20, and 30 mA. At $I_{ds} \approx 20$ mA, the FET features transit frequencies $f_t = 23$ GHz and $f_{\max} = 75$ GHz. Both $NF_{\min}$ and Rn are quite low, thus the technology is well suited for realizing low-noise MMIC amplifiers.

III. Circuit Design

The LNA consists of two stages, both transistors have a gate width of 4×50 µm. A circuit schematic is shown in Fig. 2, Fig. 3 presents a chip photo. The source of the FET in the first stage is inductively ballasted in order to improve input return loss together with noise matching. All DC bias networks are integrated on-chip. The total chip size is 3.5×1.4 mm, but the circuit has not been optimized for minimum space consumption yet.

Circuit simulation was based on small-signal analysis. The FETs were represented by measurement-extracted equivalent circuits, relying on Pospieszalski's noise model. The models of the coplanar passive elements were partly based on equivalent circuits generated from electromagnetic simulation (i.e. bends, tee-junctions, airbridges), and partly based on S-parameter measurements of test-structures (MIM capacitances, inductances).



(a)

(b)

Fig. 4. Measurement of LNA, for $V_{ds} = 8$ V for both stages, and $I_{ds} = 16$ mA and 24 mA for the first and second stage, respectively. **(a)** S-parameters and **(b)** 50 Ω noise figure NF and minimum noise figure $NF_{\min}$ of the LNA. Broken line: unstressed LNA; solid lines: stressed LNAs no. 5 and 6 (see Tab. I).

IV. Measurement Results

The LNA is designed for a supply voltage of $V_{ds} = 8$ V for both stages, with $I_{ds} \approx 16$ mA for the fist stage, and $I_{ds} \approx 24$ mA in case of the second stage, which corresponds to $\approx 12\,\%\ I_{dss}$. All measurements reported in the following refer to this bias condition.

The small-signal and noise measurements are shown in Fig. 4. Low-noise amplification is achieved in the frequency range 3.5–7 GHz, with $NF < 2.3$ dB, and $|S_{21}| > 20$ dB. In the range $f = 5$–7 GHz, $NF < 1.8$ dB is achieved, with $|S_{11}| < -5$ dB, and $|S_{22}| < -10$ dB. The lowest noise figure $NF = 1.4$ dB is measured at 6 GHz where the amplifier is matched for minimum noise. This is illustrated by Fig. 4a, where the noise figure NF of the LNA in 50 Ω environment is plotted together with its minimum noise figure $NF_{\min}$. One recognizes that for frequencies from about 5 to 7 GHz the 50 Ω results are close to the $NF_{\min}$ values, which demonstrates effectiveness of the noise matching.

To characterize the large-signal behavior, intermodula-

TABLE I

CW input power and duration of stress-tests performed with different LNA circuits. The circuits were biased for low-noise operation.

No.	P_{in}	f	time
1	20 dBm	5 GHz	10 min.
2	25 dBm	5 GHz	10 min.
3	30 dBm	2 GHz	10 min.
4	36 dBm	2 GHz	10 min.
5	27, 30, 33 dBm 33 dBm	4 GHz 4 GHz	10, 10, 10 min. 3 h 20 min.
6	30 dBm 33 dBm	2 GHz 4 GHz	20 min. 16 h
7	33 dBm 36 dBm	4 GHz 4 GHz	4 h 15 h
8	33 dBm 36 dBm	4 GHz 4 GHz	14 h 2 h 30 min.
9	33 dBm 36 dBm	4 GHz 4 GHz	2 h 30 min. 3 h 30 min.

tion distortion measurements were performed. Fig. 5 provides the relevant data. The input power was injected at $f = 5\,\text{GHz}$, with a tone-spacing $\Delta f = 1\,\text{MHz}$. According to common practice, the extrapolation of the third-order output intermodulation point (OIP3) is based on fitting lines with fixed slope of 10 dB/dec and 30 dB/dec, respectively, to the measured values. The extrapolated OIP3 is > 26 dBm. It should be noted, however, that a high linearity range was not a design goal here, only ruggedness against input overdrive. One should be able to reach much higher values of OIP3 by designing the second stage accordingly, with a larger FET biased at higher currents and voltages.

Ruggedness of the LNA was tested by injecting significant RF input power into the circuit which was biased as for normal operation. These stress-tests were carried out at the highest cw power levels reported in the literature [5], but exceeding the duration of the stressing significantly.

The tests were performed on-wafer on different circuits under the conditions listed in Tab. I. The LNA input was subjected to powers of up to 33 dBm for 16 hours, and up to 36 dBm for 15 hours at 4 GHz. At this frequency, small-signal input matching reaches almost its optimum value. Additionally, frequencies of 2 GHz and 5 GHz were applied.

The LNA is operating completely in compression at these high input power levels. As the power increases, the gate of the first stage is driven into forward bias operation due to self-biasing effects. $I_g \approx 1\,\text{mA}$ flows if 30 dBm are applied, increasing to $I_g \approx 2\,\text{mA}$ for 33 dBm, and to $I_g \approx 4\,\text{mA}$ for 36 dBm. The self-biasing behavior is identical for all input frequencies. One should note that the actual input reflection factor for such highly nonlinear operation differs considerably from the small-signal value S_{11} of the LNA.

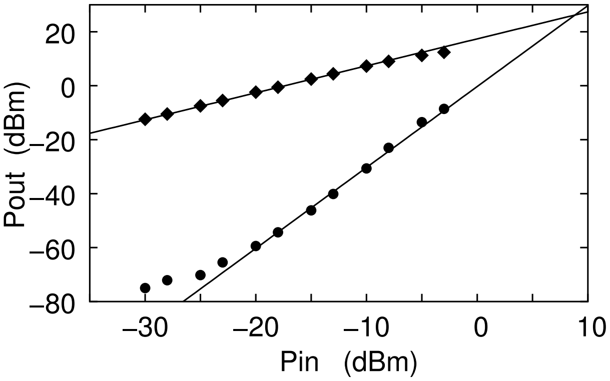


Fig. 5. Intermodulation measurement (symbols) and extrapolated OIP3 (lines) of LNA, at $f = 5\,\text{GHz}$, $\Delta f = 1\,\text{MHz}$.

None of the circuits changed its electrical properties during the measurement significantly up to input power levels of 33 dBm. Applying 36 dBm for a significant time (devices no 7–9 in Tab. I) causes a slight increase in gate current. But even in this case, no degradation is observed in terms of gain or S-parameters.

Fig. 6 shows measured S-parameters. The symbols refer to measurements performed before the circuit was stressed, the lines are obtained from measuring the same circuits after stress. It is clearly seen that the characteristics are almost identical.

An important factor responsible for poor noise performance in FETs is gate leakage current causing shot noise at the amplifier input. As the gate current irreversibly increased in the case of long-time stressing at 36 dBm, it was observed that the noise figure of these devices degraded. However, it is hardly possible to compare this result with the literature, since this information is commonly not revealed [2–5].

In the other cases, the post-stress gate currents were as low as the values measured before the stressing. While the FET of the first stage is driven into saturation during the stress measurement, causing the gate DC current to reach 2 mA, no irreversible change is observed.

Fig. 4b indicates that the stressed devices (no. 5 and 6 in Tab. I) even show an improved noise behavior comparing to an unstressed device. Also the duration of the stress (3 h 20 min or 16 h) is not important. This is, to the authors' knowledge for the first time, a verification of LNA ruggedness by post-stress noise measurements.

V. Conclusions

A highly survivable GaN-HEMT low-noise amplifier MMIC is presented in this paper. The minimum noise figure measured at 6 GHz is 1.4 dB, with $NF < 2.3\,\text{dB}$ in the frequency range 3.5–7 GHz. About 20 dB gain as well as good input and output matching are achieved.

Survivability is proven by stressing several LNA samples

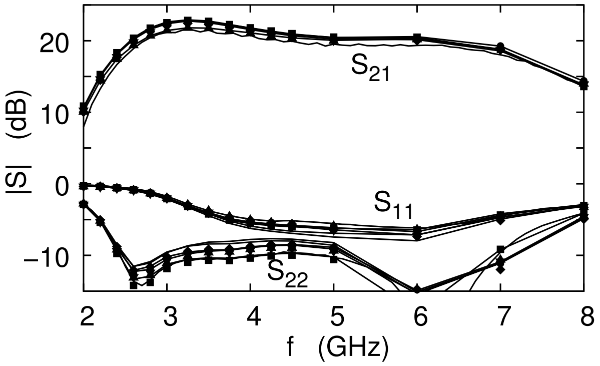


Fig. 6. *S*-parameters before (symbols) and after (lines) stressing the LNA.

biased for low-noise operation with high input power. These tests were performed at frequencies of 2, 4, and 5 GHz, with powers up to 36 dBm, for up to 16 hours. This measurement condition exceeds stress tests reported in the literature by approximately 16 hours in duration. None of the circuits degraded during the measurement up to input powers of 33 dBm. This was verified by post-stress noise, *S*-parameter, and DC measurements. Especially, no degradation of noise figure, gate leakage current, nor changes in the *S*-parameters are observed. This proves the high survivability of low-noise amplifiers in GaN-HEMT MMIC technology.

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