24 GHz Low Power VCOs and Analog Frequency Dividers

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Abstract — **24 GHz VCOs and frequency dividers with very low power consumption are presented. The circuits are realized as GaAs HBT MMICs. They comprise a VCO with high efficiency >17% and 12% tuning range at only 18 mW DC consumption as well as several frequency dividers. In order to minimize power consumption, the latter use the injection-locked frequency-divider (ILFD) concept. Divider ratios of 2 and 4 are realized, power consumption as low as 25 mW for a divider-by-2 is achieved. This demonstrates the capabilities of the analog concept in realizing dividers for mm-wave frequencies at DC consumption levels far below their digital counterparts.**

Index Terms — **VCO, Low Power, Injection Locked Frequency Divider.**

I. Introduction

RF frontends with low power consumption are finding an increasing number of applications, particularly in wireless sensor systems, in RFIDs, and for short-range communications. The low-power constraint is especially critical for frequencies above 10 GHz, where efficiency has to be sacrificed in order to meet the high-frequency performance. Among the basic building blocks of an RF frontend, the signal generation part needs special consideration. On the one hand, this is because typical efficiencies of oscillators are relatively low. Even more severe, however, is the fact that a signal source usually must contain not only a VCO but also a prescaler (or divider) providing a reference signal at a fraction of the output frequency, e.g., for stabilizing the VCO by means of a PLL. And the conventional digital dividers for mm-wave frequencies easily dominate the entire front-end in terms of power consumption.

Regarding low-power high-efficiency VCOs, several C and X-band oscillators using different technologies have been reported so far [1]-[2]-[3]. But combining very low DC power with high efficiency remains difficult because gain remains low for these bias conditions, and this becomes even worse at higher frequencies. Efficiencies are still relatively low [4]-[5] in the 20 GHz-band. Because of the small gain margin and the design requirements, using power-optimized topologies such as, e.g., class E interferes with the low power constraints.

Regarding the divider, the classical design is based on the D-Flip-Flop. These circuits are very broadband but need high power. In our case, we need the divider only to stabilize the VCO. Hence, it is not useful to be more broadband as the VCO tuning range itself. Therefore, the best solution to considerably decrease power consumption is to apply the injection locked frequency divider (ILFD) concept with one or two transistors only, which results in DC power consumptions of 20 to 30 mW compared to several 100 mW for the digital prescalers.

The purpose of this paper is to present a VCO and several dividers following the ILFD principle. The circuits operate in the 24 ISM GHz band and thus are suitable for short-range communications in this band as well as for radar sensors. Key aspects concerning efficiency optimization are discussed. In addition, we present the principle of ILFDs and design and measurements of several ultra-low power ILFDs. Key elements for ensuring low power operation and for widening the locking range such Cascode structures are highlighted. In order to fulfill the more practical condition of yield, cost, and manufacturability, a standard GaAs HBT technology is used.

The paper is organized as follows: Sec. II describes briefly the process and the modeling tools for the used technology. Sec. III presents design of the circuits. Finally, Sec. IV. is devoted to the experimental results.

II. Technology and transistor model

The HBT MMICs are fabricated on the FBH 4" process line. The epitaxial layers are grown by Metalorganic Vapor-Phase Epitaxy (MOVPE). Very high f_{max} values (beyond 170 GHz at V_{CE} =3 V) are achieved as compared to the more industry-standard f_T values (36 GHz at V_{CE} =3 V).

A customized CAD library containing both passive and active devices is used for circuit simulation. Key part is the FBH HBT model. It includes partition of intrinsic and extrinsic base-collector diode, non-ideal base currents, self-heating, base-emitter and base-collector break-down, current-dependence of base-collector capacitance $C_{bc,intr}$, and collector transit time τ_c (i.e., velocity modulation and Kirk effect, which are responsible for the f_T and f_{max} peaking).

II. Circuit Design

A. The VCO concept

In order to keep power consumption as low as possible, the circuit is designed as single transistor structure based on a series feedback topology (see Fig. 1).

The impedances formed by the short stubs on collector and base cause the transistor to be unstable and define the sharpness of the phase and hence the phase-noise value. To fulfil

the oscillation condition, the phase of the reflection coefficient on the emitter port is then equalized to zero by a varactor. The collector stub is also used for impedance matching (mainly by shifting the 50 Ohms load-impedance to lower values) and to maximize the output power. The circuit is designed so that it can operate without any resistive feedback or particular biasing topology, which would decrease the efficiency.

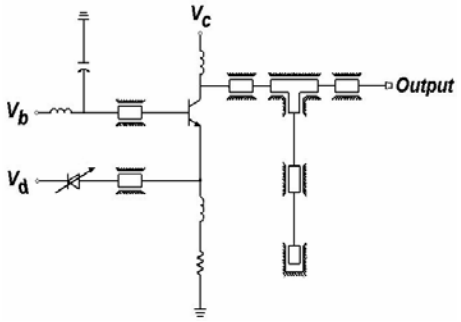

Fig. 1. Schematic diagram of the VCO

To lower the DC power, small transistors with an emitter area of 2x10 μm^2 are employed that are operated at 5 Ma bias current. This turned out to be the best trade-off between efficiency and low noise. Larger transistors would need much higher biasing currents, and even if the efficiency remains constant or is improved, they will be out of specifications in terms of low power. Smaller transistors are not interesting in terms of noise, but also, because of higher parasitic resistances, they may degrade efficiency.

Efficiency is enhanced mainly by optimizing the transistor loop gain using S-parameter simulations. Then, the harmonic-balance simulation gives the auto-biasing operating conditions to calculate DC consumption and efficiency. The best efficiency-power trade-off is obtained when the transistor is initially biased in AB class so that the loop gain starts to rise while the DC consumption is still relatively low. When the oscillations start, the collector current increases slightly but stays within an interesting region so that efficiency remains high. For lower collector currents (Class B), not enough gain is provided by the transistor to initiate the oscillations, and for higher currents (Class A), DC consumption increases while gain does not increase to the same extent, which lowers efficiency.

B. Key aspects for ILFDs design

Classical digital frequency dividers give excellent results [6] but they suffer from relatively high power consumption. The injection locked frequency divider (ILFD) topology is very well adapted to architectures with a low number of transistors, in our case, one or two transistors per divider stage.

The main problem of analog, often also called regenerative dividers, is their limited locking range. Several publications have proposed analytical approaches to predict the locking ranges of these circuits [7]-[8]. ILFDs are generally modelled by a nonlinear function followed by a filter (see Fig. 2).

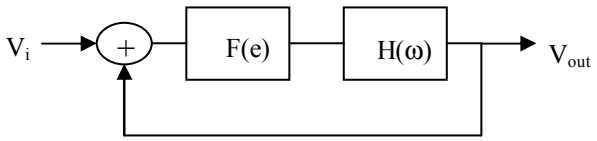

Fig. 2. Equivalent diagram of an ILFD.

Using this model, and under certain conditions [7], the locking range of such a divider is given by the relation

$$\left|\frac{\Delta\omega}{\omega_T}\right| = \left|\frac{H_0 \cdot a_2 \cdot V_{input}}{2Q}\right|,$$

where $\Delta\omega$ denotes the locking range, ω_T and Q the resonant frequency and quality factor of the equivalent RLC circuit of the oscillator, respectively (the ILFD in this case). a_2 is a parameter of the nonlinear function F(e), and H_0 is the magnitude of the transmission function H(ω).

One can then see two ways of increasing the locking range: Either one increases the value of H_0/Q. This is a good solution for our application because it fits the low power specifications. The limit is given by the resonance frequency of the inductor itself: increasing H_0/Q means having a larger value of L ($H_0/Q=L\omega$). The other point is that the phase condition must be always fulfilled (also without input signal). Having too large inductors can fail to satisfy this condition.

The second solution is, of course, simply to increase the input voltage. In our case, we want to have low input signal amplitudes so that the dividers can be used with the designed VCOs. So this solution is not attractive, but actually leads us to fix one aspect of the architecture: larger input voltage amplitudes lead to wider locking ranges. This means the input of the ILFD must be at a high impedance node, typically the base.

One other important point has to be noticed: These calculations rely on the assumption that input and output are perfectly isolated, or that the only correlation between them is described by the nonlinear function F(e) and the filter. This means that enhancing this function (i. e., increasing a_2, the nonlinear factor, increases the locking range as well). Also, this means that parasitics will cause a decrease in locking range. Therefore, high-isolation architectures such as Cascode structures are to give better results than those with a single transistor [7].

C. Designed ILFDs

The dividers are designed following the same steps as for the VCO at 12 and 6 GHz for division ratios of 2 and 4 respectively. Three versions of ILFDs were designed. The two first ones have a division ratio of 2 and use 2x10 um^2 emitter-area transistors. The last one has a division ration of 4 and uses a 3x30 um^2 emitter-area transistor. For all three, the input is at the base (of the bottom transistor for the Cascode circuit). They are all three based on reflection-type oscillators. The first one was optimized with regard to locking range. It uses a Cascode-based reflection VCO at 12 GHz. The second one

was optimised with regard to power consumption. A particularly small transistor is used and operated in class AB.

At the input, a λ/2 transmission-line is added to present a ground to the resonant circuit on the base at the first harmonic (12 or 6 GHz). From the low-power point of view these circuits have been optimized in the same way as the VCO was treated trying to establish class AB operation. These circuits have been simulated using harmonic balance, optimizing the high harmonics of the signal to increase locking behaviour on the input signal at $2f_{0SC}$ or $4f_{0SC}$.

IV. Experimental Results

A. *Low power high efficiency VCO*

The VCO was measured using on-wafer 50 ohms probes and a spectrum analyzer. As predicted by the harmonic balance simulation, oscillations start at a collector voltage as low as 1.5 V for a 5 mA collector current. Two collector voltages are chosen, 2 V and 2.5 V. For each, the collector current is increased by the means of the base voltage, changing the operation point from class B via AB to A. As predicted by the simulation, oscillations start at the transition between class B and AB. Efficiency increases slightly to a maximum value (located in the class AB region), or oscillations start directly at the maximum efficiency value for the case with Vce=2.5 V, and efficiency then decreases when entering the pure class A. For 18 mW of DC consumption (2.5 V x 7 mA) the VCO delivers 5 dBm output power, which yields a collector efficiency of slightly more than 17%.

The frequency could be tuned from 22.8 up to 25.7 GHz which corresponds to a 2.9 (12%) tuning range with 1 dB variation in output power.

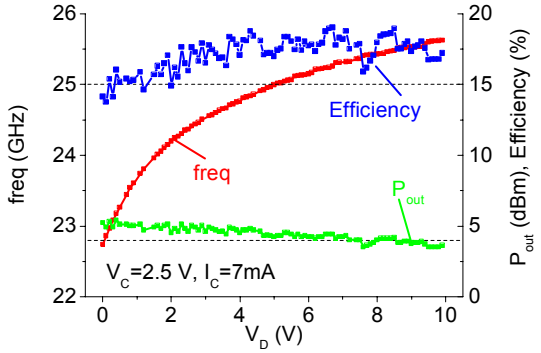

Fig. 3. *Measured tuning range, efficiency, and output power of the VCO.*

Subsequently, phase noise measurements were performed with the EE5504 Agilent system applying the delay line method. A phase noise of –64 dBc/Hz is measured at 100 kHz offset frequency under free running conditions.

B. *Low power divider*

The circuit was measured first under free running conditions. It shows an oscillation frequency of 12.3 GHz and an output power of 5 dBm for 25 mW consumption (2.5 V x 10 mA). Then, a signal is applied at the input with two power values, 0 and 6 dBm, at 24 GHz performing a frequency sweep. As long as the output frequency follows the input frequency, one is within the locking range. In this case, only two frequencies are seen on the spectrum analyser output (see Fig. 4). When the input frequency is out of the locking range, the ILFD goes back to its free running frequency and mixing is observed (see Fig. 5).

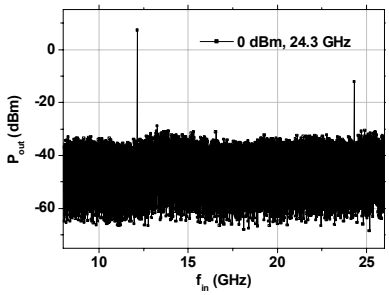

Fig. 4. *Output spectrum of the ILFD within the locking range (0 dBm input signal).*

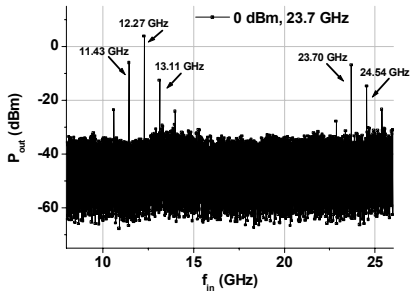

Fig. 5. *Output spectrum of the ILFD outside the locking range (0 dBm input signal).*

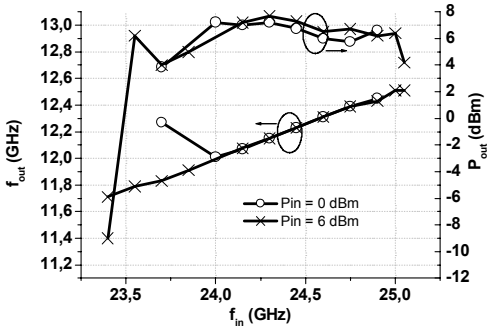

Fig. 6. *Measured output power and locking range of the low power ILFD.*

Fig. 6 summarizes the results. One can see that the output power does not depend on the input power, because it is generated by the circuit itself. To further check locking characteristics of this circuit we measured the phase noise at its output if no signal is applied at the input and if a signal is applied. The free running output exhibits a phase noise of -65dBc/Hz

at 100 kHz offset frequency. When applying a signal with -94 dBc/Hz phase noise at the input at the same offset frequency, the output noise falls to -103 dBc at 100 kHz offset frequency (see Fig. 7). This proves that the ILFD is correctly locked to the input signal.

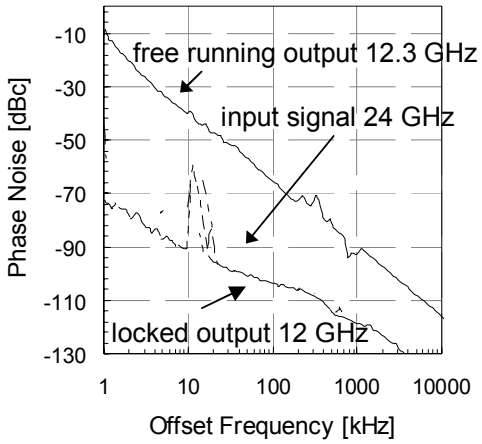

Fig. 7. *Measured phase noise against offset frequency (input signal at 24 GHz, output free running signal at 12GHz, locked output signal at 12 GHz).*

C. Cascode based ILFD

This circuit shows a free running frequency around 12 GHz with –10 dBm output power and a consumption of 40 mW (5Vx8 mA). The locking range was measured applying an input power of 0 dBm. The circuit shows a much larger locking range of 2.3 GHz compared to the one-transistor based ILFD. This improvement in locking range can be explained by the better isolation between input and output.

C. ILFD with a division ratio of 4

This case is of particular interest because the larger division ratio allows for a reduction of divider stages. The free running oscillation frequency was around 6 GHz. The power consumption of this circuit was higher than the two others because a larger transistor is used (but this is, of course, offset by a potential reduction in the number of divider stages): The transistor was operated at 3 V V_{ce} and a current of 20 mA, thus DC consumption is 60 mW, which is an excellent value compared to other divider solutions. Under these conditions, the output power was 4 dBm. For 0 dBm input power, a locking range of 1 GHz was observed ranging from 23.9 to 24.9 GHz.

As for the other dividers, noise measurements were performed in order to check the divider function. Under free running conditions, the output signal at 6 GHz shows a phase noise of -71.2 dBc/Hz at 100 kHz offset frequency. When applying a 24 GHz signal at the input with -97.3 dBc/Hz, the divider output gets locked and noise drops to -110 dBc/Hz. This value corresponds to the expected behavior: for a division ratio of 4, the output noise should be 12 dB lower than the input noise, plus the noise contribution of the divider, which is less than 1 dB here.

IV. Conclusion

Low power building blocks for signal generation at 24 GHz are presented: On the one hand, a low-power high-efficiency VCO with only 18 mW DC consumption and 17 % efficiency; on the other hand, the injection-locking principle is used to realize regenerative frequency dividers with minimum power requirements. Excellent results are obtained, a divider by 2 consuming no more than 25 mW, and a circuit with a division ratio of 4 operating at only 60 mW DC power.

These results prove the feasibility of realizing low-power signal generation units also at mm-wave frequencies. The frequency dividers open also inexpensive and compact possibilities of stabilizing VCOs at very high frequencies, for which digital prescalers are not available or too expensive.

References

[1] Ellinger, F., Lott, U., Bachtold, W., “Design of a low-supply-voltage high-efficiency class-E voltage-controlled MMIC oscillator at C-band“, Trans. on Micro. Theory. and Tech., VOL. 49, Jan. 2001, pp. 203 - 206.

[2] De Los Santos, H.J., Chui, K.C., Chow, D.H., and Dunlap, H.L., “An efficient HBT/RTD oscillator for wireless Applications”, IEEE Microwave and wireless components letters, VOL. 11, May 2001, pp. 193 - 195.

[3] Tsang, T.K.K., El-Gamal, M.N., “A high figure of merit and area-efficient low-voltage (0.7-1 V) 12 GHz CMOS VCO”, Radio Frequency Integrated Circuits (RFIC) Symposium, June 2003, pp. 89 - 92.

[4] Hayama, N., Shimizu, J., and Honjo, K., “Fully monolithic 22 GHz-band AlGaAs/GaAs HBT oscillator”, Electron. Lett., Sept. 1991, pp. 1862 - 1863.

[5] Donghyun, B., Jeonggeun, K., Songcheol, Ho., “A dual-band (13/22-GHz) VCO based on resonant mode switching”, IEEE Microwave and Wireless Components Letters, Vol. 13, Oct. 2003, pp. 443 - 445.

[6] M.Schott, F.Lenk, C.Meliani, and W. Heinrich, « Low Phase Noise X-Band Push-Push Oscillator with Frequency Divider », in Proc. IMS 2005, Long Beach, CA.

[7] H. R. Rategh, and T. H. Lee, « Superharmonic Injection-Locked Frequency Dividers », IEEE Journal of Solid-State Circuits, Vol. 34, June 1999, pp. 813 – 821.

[8] Kwok-Keung M. Cheng, and Chun-Wah Fan, “A Novel Approach to the Analysis of Microwave Regenerative Analog Frequency Dividers”, IEEE Microwave and Guided Wave Letters, Vol. 8, July 1998, pp. 266 - 267.