A 24 GHz Active Antenna in Flip-Chip Technology with Integrated Frontend

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***Abstract* — A novel slot antenna is presented which is realized using flip-chip technology and allows integration of active chips into the antenna. It is compatible with conventional planar assembly methods and exhibits resonant properties that can be used as an input/output filter. Combining 4 antennas one obtains a compact module with beam switching in all lateral directions. For 24 GHz, only 12 mm side length are required. The paper describes antenna design and presents measurement results of a 24 GHz version with integrated transmitter VCO.**

***Index Terms* — Slot antenna, flip-chip, sector antenna, planar integration, resonant antenna.**

I. Introduction

Future applications in sensor networks and short-range communications demand for compact antennas that can be integrated with the frontend circuit. For specific systems, even a directional radiation would be useful, which allows a certain beam steering thus saving on energy or selecting an individual partner node in a network. The antenna must be compact, mechanically stable and compatible with the conventional assembly and integration methods. The conventional solution to this problem is the patch antenna [1,2]. However, it must be located on top of a planar circuit board and, hence, does not allow radiation in lateral directions. The slot antenna presented here [3] represents the ideal complement because it radiates laterally and offers additional features such as beam steering and filtering.

The purpose of this paper is to explain the design parameters and to demonstrate that it can be realized as an active antenna with a GaAs VCO chip integrated into the antenna. The paper is organized as follows: The first part describes the antenna basics (Sec. II), the second part (Sec. III) is devoted to the specific assembly with integrated chip, covering design issues as well as packaging technology and realization (Sec. IV).

II. Antenna Basics

Fig. 1 illustrates the geometry of the slot antenna. It consists of an upper and a lower substrate stack which are flip-chip mounted face-to-face. In this way an air gap as thick as the bump height is created, which is used here as a parallel-plate geometry to guide waves and to radiate them through the slot at the outer edges. Bump fences separate the different sectors from each other and direct the beam. Within the lower and upper substrate, via fences have to be used to suppress resonances and to shield the substrates against radiation from outside. Fig. 1 shows the resulting structure with a 4-quadrant antenna. The via fences along the outer edges perform the shielding of the substrates.

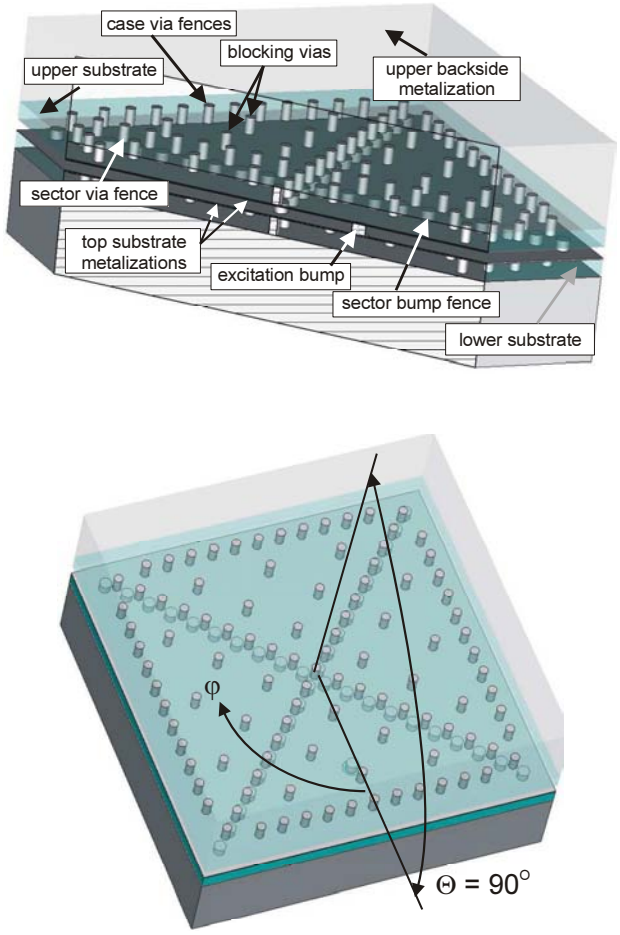

Fig. 1 : Geometry of the slot antenna

The lower and upper substrates are complemented in Fig. 1 by metallic blocks, which in reality can contain a further stack

of substrates with low-frequency electronics or other components such as batteries. The only condition is that these blocks need via fences or similar arrangements at the sides to shield them against RF radiation from the slot.

One sector of the 4-quadrant slot antenna in Fig. 1 can be understood as a triangular cavity with an open slot at the outer side. This cavity is excited by a bump near the center of the cavity. Because of the relatively low cavity height there is a strong mismatch between the cavity impedance and that of the outer space. Therefore, the cavity is operated near resonance, which allows impedance transformation and results in a resonant antenna with filtering properties. Fig. 2 presents the frequency dependence of the input reflection factor at the excitation bump (simulation results assuming a lossless structure). One observes a relatively narrow filter curve, whose center

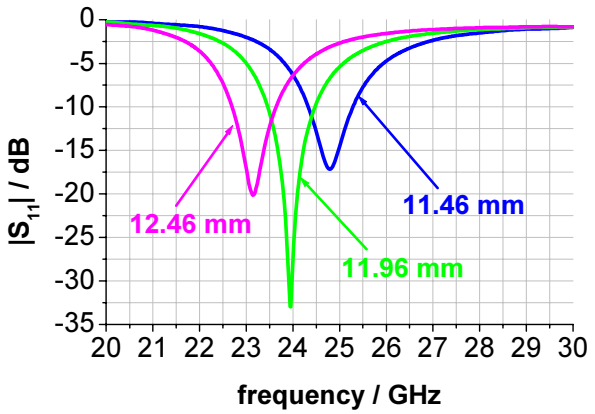

Fig. 2 : Input reflection factor of one segment of the antenna against frequency with the outer dimension as a parameter (antenna as in Fig. 1, port at the excitation bump, simulation results for lossless antenna).

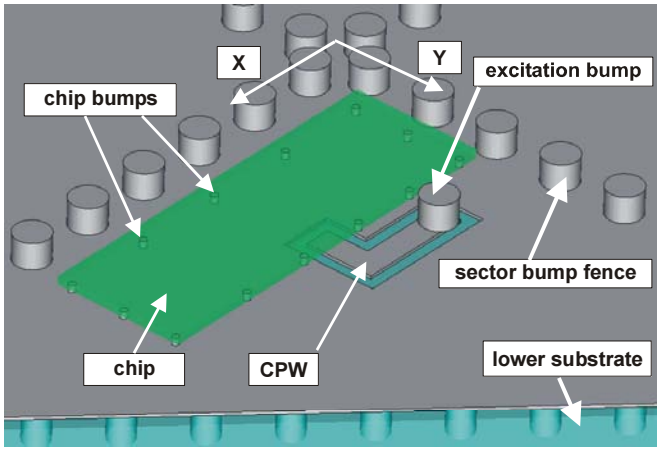

Fig. 3 : View to the environment of the integrated chip

frequency is related to the cavity dimensions (i.e., the outer dimension of the antenna). For the 24 GHz band, side lengths around 12 mm are necessary, which results in a rather compact design. In reality, bandwidth increases due to the losses, of course. Besides the outer dimensions of the antenna, other parameters such as bump height and the actual geometry at the outer edges (the substrate and the via fences) influence the frequency characteristics [4,5]. This has to be taken into account by means of em simulation. In our case, the basic antenna geometry was designed for a frequency of 24 GHz (ISM band). The simulations were performed using the FDTD software MWS from CST [6].

In the intended active antenna configuration, the active chips are to be integrated into the cavity. This is described in the next section.

III. Antenna with Integrated Chip

Integrating chips into the antenna cavity needs specific design and processing efforts. Fig. 3 illustrates how the chip is located inside the antenna. Flip-chip mounting is used. Of course, the resulting thickness of the chip must be smaller than the height of the cavity, which means that flip-chip processes with two different bump sizes have to be used.

Clearly, the chip will disturb the fields inside the cavity of the slot antenna. In more detail, one has the following effects

- dielectric loading due to the high dielectric constant of the chip (GaAs, $\varepsilon_r = 12.9$).
- the feeding lines (CPW) contain gaps which interrupt the current flow of the ideal slot antenna.

Accordingly, simulations were carried out to optimize the orientation and location of the chip, to find the best position for the excitation bump, and to route the CPW line from the chip to the excitation bump in a way, which does not disturb the surface current flow on the antenna too much. Moreover, one has to make sure to place some more vias in the substrate surrounding the CPW in order to suppress resonances in the substrate excited through the CPW gap. Fig. 4 shows how shifting of the excitation bump along with the CPW in y-direction (see Fig. 3) influences resonant frequency and impedance matching. One sees that varying its position these two properties can be optimized.

Fig. 5 illustrates how the chip perturbes the current flow in the antenna. For this purpose, two different chip layouts are compared, a fully metalized surface and a pattern with a slot preventing currents transverse to the CPW slots. As can be seen from Fig. 5(b) the latter case leads to a decrease in resonant frequency.

As substrate material, we use Rogers 4003 ($\varepsilon_r = 3.38$) of 508 µm thickness with a 35 µm top metalization. Accordingly, the substrates are structured using a standard hybrid softboard process, which is cost-effective but involves relatively large tolerances. They have to be accounted for in antenna design.

For chip mounting, we apply AuSn ball bumps of 80 µm diameter, which are deposited by a ball bumper. The bumps need to be placed on the chip because lateral alignment is most

critical here. Then, the chip, together with the balls, is flip-chip mounted onto the Rogers substrate by solder bonding.

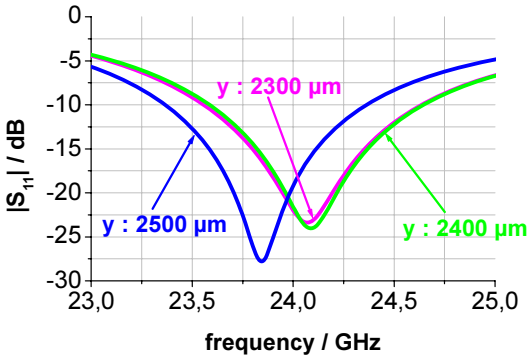

Fig. 4 : Influence of excitation bump position according to Fig.3. (bump position in x = 1300 µm)

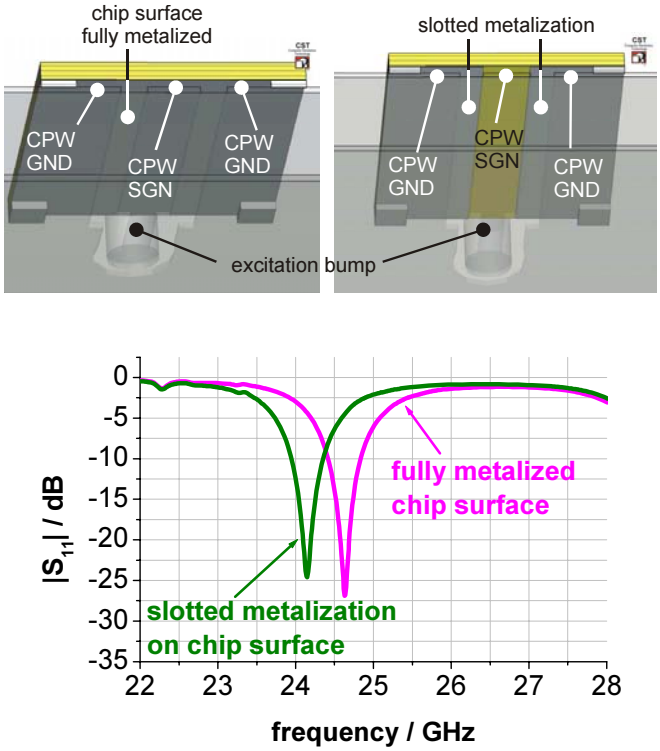

Fig. 5: Chip with fully metalized surface and with slotted metallization (top); reflection factor for both cases (bottom).

A similar process is applied to flip-chip mount the lower substrate with the chip to the upper substrate. But, larger bumps are needed to maintain enough margin so that the height of the lower substrate with the mounted chip is small enough compared to the resulting bump height of the second flip-chip process. Therefore, we use 400 µm balls for this process, which defines the height of the antenna cavity. The tolerance in nominal height (300 µm) of the antenna slot is about 15…20 µm.

IV. Realization

Fig. 6 (a) presents a photograph of the lower Rogers board after mounting the chip. In our case, it is a GaAs VCO. Surrounding the excitation bump one can see some additional vias in the Rogers substrate and the sector via fences.

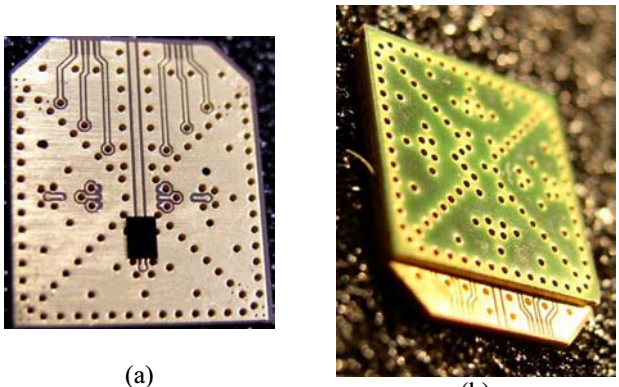

Fig. 6 : Photographs of realized boards with integrated chips.

The completed antenna after the second flip-chip process is shown in Fig. 6 (b). The lower board is extended on one side to allow on-wafer probing or bonding of the feeding lines. Clearly, the vias in the Rogers substrate can be seen, which are realized as through-vias here. They are located along the outer edges of the substrate for shielding purposes as well as inside. There, the diagonal fences separate the four sections from each other and the remaining vias are distributed in a way to suppress substrate resonances.

First, we measured a device according to Fig. 6 with a CPW feeding line and a dummy chip above this line. This allows easy connection to a wafer prober or an SMD connector (see vertical CPW in Fig. 6 (a)). Measured data for this device is plotted together with simulations (lossless structure) in Fig. 7. Qualitative agreement is good, but the measured curve is about 3 dB lower than the simulated one. This can be explained by the conductor loss on the CPW feeding line (appr. 10 mm long) and in the antenna.

In order to further characterize the loss and to determine antenna efficiency, we positioned two such antennas face-to-face a few millimeters apart and measured transmission loss. A loss value per antenna of 3dB was obtained, which corresponds to 50%. Together with a calculated directivity of 7 dB this yields 4 dB of gain. We performed measurements with two antennas at distances between 3…30 cm in order to verify this experimentally. The measurements yield a similar gain value but, due to the small size of the antenna, the uncertainties of such a

relatively simple measurement setup reach several dB and thus are not sufficient for an exact validation.

In order to demonstrate functionality of the active antenna, we realized a complete antenna with an integrated GaAs-HBT VCO. The MMIC chip was fabricated using the FBH GaAs-HBT process. Chip size and layout are adapted to meet the constraints given by the antenna integration. It is a coplanar circuit with a 100 µm thick substrate.

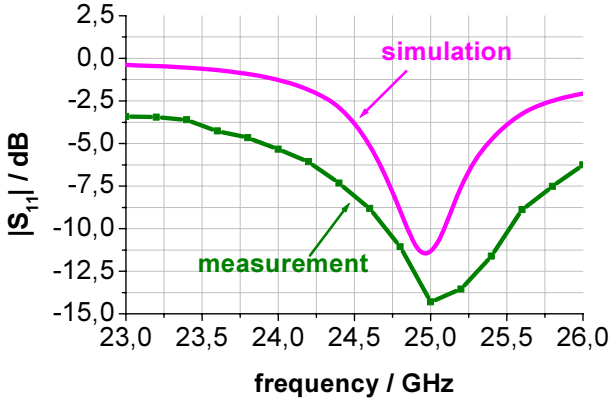

Fig. 7: Input reflection factor against frequency for the device in Fig. 6 using the CPW feed line; comparison between measurements and simulation (lossless).

The antenna with the VCO was mounted on a probe station with the appropriate DC bias and control signals applied by a probe card. The radiated signal was detected by a horn antenna as a receiver. Fig. 8 illustrates the measurement set-up.

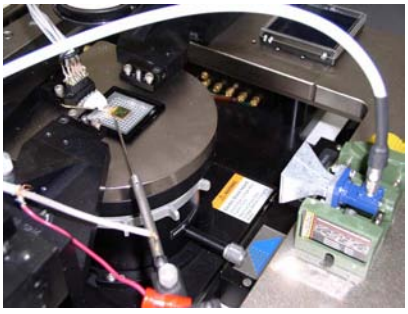

Fig. 8 : Measurement set-up for the active antenna with horn antenna as a receiver.

The results of this measurement are depicted in Fig. 9. What is plotted is the frequency of the received signal at the horn antenna when varying the tuning voltage and thus frequency of the VCO in the active slot antenna. An almost linear tuning range from 23.3 GHz to 25.0 GHz is observed. This proves functionality of the active antenna concept.

In the final realization, the transmitter VCO is to be realized on a single chip together with a mixer and an LO, which forms a complete RF frontend. Then, bias supply as well as the IF signals can be fed through vias from the backside so that the four sections can be operated independently.

V. Conclusion

An active 4-quadrant slot antenna for the 24 GHz range is described. It is based on a two-step flip-chip process. The antenna includes resonant characteristics, which may be used for filtering purposes. A first realization with a transmitter VCO is demonstrated. The antenna allows integration of the complete RF frontend, which leads to very compact modules, particularly suitable for sensor networks.

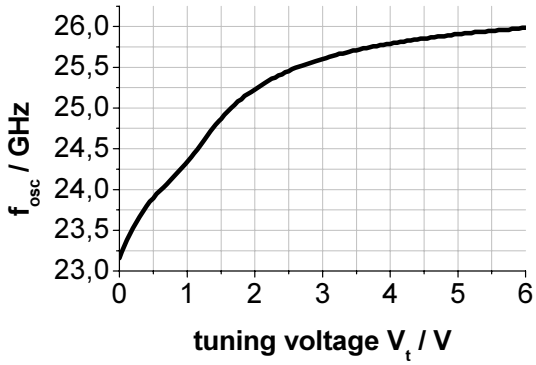

Fig. 9 : Measured frequency at the horn-antenna receiver as a function of tuning voltage of the active antenna (set-up according to Fig. 8).

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