Laser-Assisted Processing of VIAs for AlGaN/GaN HEMTs on SiC Substrates

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***Abstract*—Vertical interconnect accesses (VIAs) were fabricated between the source electrode on the front and the ground on the backside of high-power microwave AlGaN/GaN high-electron mobility transistors (HEMTs) on $\sim$ 400-μm-thick silicon carbide substrates. Through-wafer microholes with an aspect ratio of up to $\sim$ 8 were drilled using pulsed UV-laser machining and subsequently metallized using electroplating. The successful implementation of the laser-assisted VIA technology into device processing was proven by dc and RF characterization. When biased at 26 V, a saturated output power of 41.6 W with an associated power-added efficiency of 55% at 2 GHz was achieved for a 20-mm AlGaN/GaN HEMT with through-wafer VIAs.**

***Index Terms*—GaN, high-electron mobility transistor (HEMT), laser machining, laser materials-processing applications, semiconductor device fabrication, silicon carbide (SiC) substrate, vertical interconnect accesses (VIAs).**

I. INTRODUCTION

AlGaN/GaN-based high-electron mobility transistors (HEMTs) have attracted much attention due to the material's superior electronic properties for RF and microwave power devices both for military and commercial applications [1]. Best power performance has been achieved for AlGaN/GaN HEMTs on silicon carbide (SiC) substrates [2], [3]. To create low-inductance ground connections to the source pads using vertical interconnect accesses (VIAs) microholes have to be processed in the chemically inert and very hard SiC. Currently, there is no feasible technology known for processing VIAs through 400-μm-thick semiinsulating SiC. Such a technology would allow simplified device mounting and space-saving design strategies. Due to the low etching rate of ≤ 1 μm/min even in advanced inductively coupled plasma, the formation of microholes using conventional lithography and plasma processing requires a time-consuming preparation by thinning of the SiC substrates to ~ 100 μm [4]. In this letter, we report on a direct UV-laser micromachining of through-wafer microholes and its implementation into the fabrication of VIAs for advanced high-power AlGaN/GaN HEMTs on 400-μm SiC substrates. Neither time-consuming wafer thinning nor backside lithography is necessary to form the holes. The compatibility of laser microablation with a semiconductor device fabrication will be demonstrated.

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II. EXPERIMENTAL

The laser-assisted VIA technology was tested and implemented in back-end processing of AlGaN/GaN power transistors. The $\sim$ 2.5-μm AlGaN/GaN HEMT structures were grown by metal–organic vapor-phase epitaxy on $\sim$ 400-μm semiinsulating SiC. The 2-in wafers received the complete process on the front using 0.5-μm stepper lithography [5]. The source pad metal of the transistors consisted of Ti/Pt/Au layers.

A frequency-tripled diode-pumped solid-state laser providing 4.5 W average power at 25-kHz pulse repetition rate and a pulselength < 30 ns was used for laser drilling. The laser is integrated into an industrial-grade micromachining workstation (ILS 500 Air, InnoLas) that is equipped with an air-bearing XY stage and galvo-scanning optics. The 355-nm laser beam is focused using a flat-field (f-theta) lens having a focal length of 56 mm. The microholes are drilled by the laser from the substrate's backside through the source pads. An automated beam alignment provides a positioning accuracy of the laser beam (on the backside) with respect to existing transistor patterns (on the front) of ± 1 μm [6].

Prior to laser drilling the front of the AlGaN/GaN power transistors except for the source pads that are drilled through was protected by photoresist. The holes were drilled one at a time in ambient atmosphere. To obtain the desired hole diameter the beam was circularly scanned. Pulse energies of $\sim$ 65 μJ/pulse at 20-kHz pulse repetition rate were used to create through-wafer microholes. Depending on the transistor size and layout up to 22 VIAs were drilled into a single power bar. Without having optimized the drilling process for a high throughput, the processing time for a 50-μm hole through 400-μm SiC is $\sim$ 3 s, i.e., within 3 h time, we can drill $\sim$ 3600 holes that are required for processing a typical 2-in wafer with AlGaN/GaN power bars. The holes are conical and have smooth sidewalls that are covered by a thin layer of resolidified material [6]. After etching in hydrofluoric acid to remove ablated matter deposited near the holes a Ti/Au plating base was evaporated onto the wafer's backside including the tapered sidewalls of the holes. Subsequently, the metal layer was thickened by electroplating 5 μm of gold. During electroplating, both sides of the wafer are in contact with the electrolyte, i.e., the electrolyte can flow through the holes and the gold layer grows also on the unprotected source pads.

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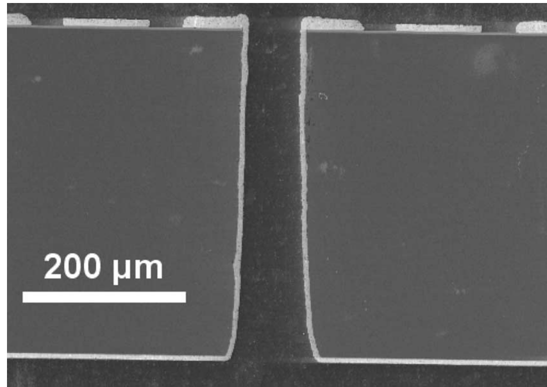

Fig. 1. Cross-sectional SEM image of a source VIA in semiinsulating SiC with AlGaN/GaN HEMT structure (top). The hole was drilled by the laser from the bottom and then gold plated.

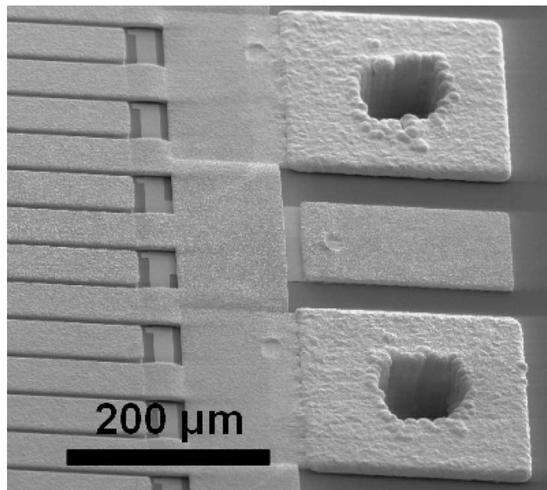

Fig. 2. SEM image of a detail of an AlGaN/GaN transistor structure with through-wafer source VIAs after gold plating. The source pads were not protected by photoresist during laser drilling and electroplating. Therefore, the gold layer is thicker on these pads and there are small steps in the contact stripes.

Before wafer dicing and chip mounting, a titanium dewetting layer was deposited onto the VIAs' sidewalls to prevent the solder from flowing through the open holes due to capillary effects and splashing onto the front. VIAs with aspect ratios of up to ~ 8 have been realized.

On-wafer pinchoff tests, as well as dc and load-pull measurements [7], were performed before and after laser drilling. After dicing the wafer, transistors were mounted into standard microwave packages by AuSn soldering for RF characterization.

III. Results and Discussion

Fig. 1 shows the cross section of a transistor on semiinsulating SiC with a plated-through hole. At the top there is the transistor's source pad that is drilled through. The gold layer is completely closed and has a homogeneous thickness of $\sim 5\ \mu$m throughout the hole. Resistance measurements have proven that a reliable electrical connection was established between front and backside (bottom). The typical electrical resistance through a single VIA having an aspect ratio of ~ 4 is < 17 mΩ. In Fig. 2, a detail of an AlGaN/GaN transistor device processed with through-wafer VIAs is shown.

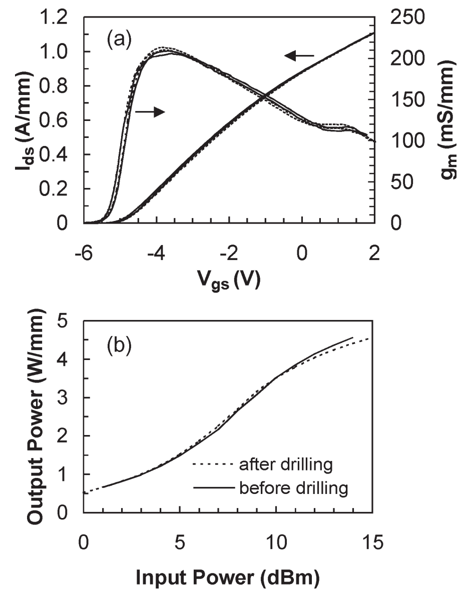

Fig. 3. Electrical on-wafer measurements were performed before (solid lines) and after laser drilling (dotted lines) of VIA holes at a distance of $\sim 3\ \mu$m from the active device region (gate finger): (a) dc transfer characteristics of a 2×125-μm transistor device at a drain source voltage of 15 V, transconductance (g_m), and drain–source current ($I_{\rm ds}$) versus gate–source voltage ($V_{\rm gs}$). (b) RF output power characteristics of a 2×125-μm transistor device measured at 2 GHz as a function of the input power (load pull).

In order to check for a potential degradation of transistor performance due to laser processing, on-wafer dc and load-pull measurements were performed before and after laser drilling. In Fig. 3, results are presented for transistors with two gate fingers and a gate width of 125 μm before and after drilling holes $\sim 3\ \mu$m beside the gate fingers. Typical values of the two-finger transistors in this letter were: threshold voltage $V_{\rm gs} = -5$ V, maximum drain-source current $I_{\rm ds} = 300$ mA (1.2 A/mm), maximum transconductance $g_m = 200-240$ mS/mm, output power 5 W/mm, 20 dB of gain. Within the error limits the corresponding curves do not differ from each other indicating that there is no collateral damage due to laser processing. Work is currently in progress to explore the minimum distance that is possible between the laser drilled VIA hole and the active transistor region.

Load-pull measurements were performed in a power transistor fixture for power transistors that comprises two microstrip circuits for input and output matching of the different types of transistors. Additional fine-tuning was achieved using external slide-screw tuners. As an example the power performance of a device having a total gate width of $5 \times 8 \times 500$-μm device is shown in Fig. 4. The distance between the VIAs and the active gate region of the device were $\geq 120\ \mu$m. The continuous wave (CW) power sweep at 2 GHz measured at room temperature demonstrates 13.8 dB of linear gain and a saturated output power of 41.6 W. The device was operated at a drain-source bias of $V_{\rm ds} = 26$ V and a quiescent current of $I_{\rm dq} = 1.6$ A. At an input power level of 35.3 dBm, the output power reached 46.2 dBm with an associated power-added efficiency (PAE) of 55.3%.

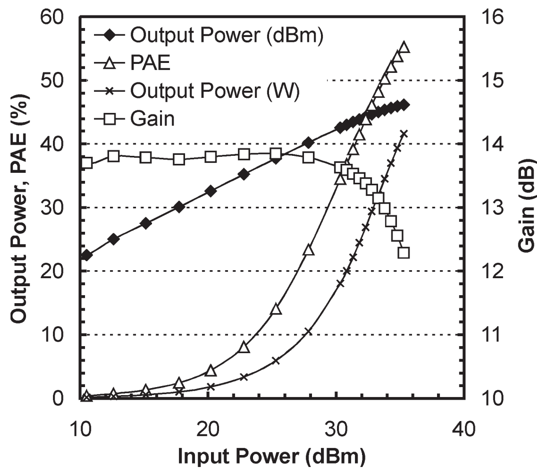

Fig. 4. Power performance at 2 GHz for a $5 \times 8 \times 500$-μm AlGaN/GaN HEMT power bar (five cells with eight gate fingers each, gate width 500 μm) on SiC with ten through-wafer source VIAs when biased at 26 V and 1.6 A. A saturated output power of 41.6 W with an associated PAE of 55.3% was achieved.

Computer simulations of the heat conduction using the finite element method revealed that maintaining the full thickness of the SiC substrate helps heat spreading and does not compromise thermal resistance $(R_{\rm th})$. The device consisting of 12 gate fingers each having a gate width of 125 μm was assumed to be mounted on CuW using 20-μm-thick Au/Sn solder. For a 350-μm-thick SiC substrate, $R_{\rm th} = 9.4$ K/W was calculated compared to $R_{\rm th} = 9.7$ K/W for a 100-μm-thick substrate, which correspond to maximum channel temperatures of 417 and 420 K, respectively. Although the numerical results do depend on the specific transistor layout and assumptions about material parameters, the ratio of the channel temperatures should not significantly change. Due to the very high thermal conductivity of SiC, the heat is spread in the substrate above the solder layer having a much smaller thermal conductivity. The overall thermal resistance is limited by the 20-μm-thick solder layer and cannot be reduced by thinning the SiC substrate.

IV. Conclusion

Laser-assisted processing of through-wafer VIAs was successfully demonstrated for high-power AlGaN/GaN HEMTs on 400-μm-thick semiinsulating SiC. Computer simulations revealed that the thermal resistance of the mounted chip using 20-μm Au/Sn solder is limited by the solder and not by the thickness of the SiC. Compared to plasma processing, the laser-assisted VIA process does not require the time-consuming wafer thinning and backside lithography. VIAs having an aspect ratio of ~ 8 were fabricated to connect the source contacts on the front to the ground at the backside of the devices. No degradation of device performance due to laser processing was found by on-wafer dc and RF measurements. With power bar devices, a CW power of 41.6 W with an associated PAE of 55.3% was achieved at 2-GHz and 26-V drain bias. The results demonstrate the compatibility of the laser microablation with the semiconductor device fabrication. Direct laser micromachining can be a promising alternative to conventional lithographic and plasma microprocessing of hard and inert materials.

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References

[1] U. K. Mishra, P. Parikh, and Y.-F. Wu, "AlGaN/GaN HEMTs—An overview of device operation and applications," *Proc. IEEE*, vol. 90, no. 6, pp. 1022–1031, Jun. 2002.

[2] Y.-F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30-W/mm GaN HEMTs by field plate optimization," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 117–119, Mar. 2004.

[3] T. Kikkawa, E. Mitani, K. Joshin, S. Yokokawa, and Y. Tateno, "An over 100-W CW output power amplifier using AlGaN/GaN HEMTs," in *Proc. GaAs MANTECH Int. Conf. Compd. Semicond. Manuf. Technol.*, 2004, pp. 97–100.

[4] J. W. Palmour, S. T. Sheppard, R. P. Smith, S. T. Allen, W. L. Pribble, T. J. Smith, Z. Ring, J. J. Sumakeris, A. W. Saxler, and J. W. Milligan, "Wide bandgap semiconductor devices and MMICs for RF power applications," in *IEDM Tech. Dig.*, Washington, DC, Dec. 2–5, 2001, pp. 17.4.1–17.4.4.

[5] R. Lossy, N. Chaturvedi, P. Heymann, K. Köhler, S. Müller, and J. Würfl, "AlGaN/GaN HEMTs on silicon carbide substrates for microwave power operation," in *Proc. GaAs MANTECH Int. Conf. Compd. Semicond. Manuf. Technol.*, Scottsdale, AZ, May 19–22, 2003, pp. 327–330.

[6] O. Krüger, G. Schöne, A. Liero, J. Würfl, and G. Tränkle, "Laser drilling of microvias in silicon carbide for AlGaN/GaN power transistors," in *Proc. 3rd Int. WLT Conf. Lasers Manuf.*, E. Beyer, F. Dausinger, A. Ostendorf, and A. Otto, Eds, Munich, Germany, Jun. 2005, pp. 663–667.

[7] P. Heymann, R. Doerner, and M. Rudolph, "Harmonic tuning of power transistors by active load-pull measurement," *Microw. J.*, vol. 43, no. 6, pp. 22–37, 2000.