Low Phase Noise X-Band Push-Push Oscillator with Frequency Divider

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Abstract— **A MMIC Colpitts oscillator in push-push configuration with integrated frequency divider using InGaP/GaAs HBTs is presented. The output is taken from the second harmonic port while the fundamental signal is fed to a frequency divider by two thus providing a reference signal at one quarter of the output frequency. The MMIC VCO reaches state-of-the-art phase-noise performance in X-band down to -120dBc/Hz at 1MHz offset frequency at high output power and a tuning range of 4%.**

Keywords—**Colpitts oscillator, Push-Push**

I. INTRODUCTION

The push-push principle is widely accepted as an approach to realize low phase-noise high-frequency oscillators. Mostly, however, it is applied in conjunction with oscillators based on a T-configuration of the feedback network and not a Π structure as in the Colpitts oscillator. This is not surprising because of the following reasons:

- The maximum oscillation frequency is lower in the Π case since the transconductance is short-circuited.
- The feedback elements are placed in series with the transistor nodes in the T-configuration, which relaxes layout constraints. Arranging feedback elements in parallel often requires the transistor cell to be modified.

Despite of these problems, the Colpitts oscillator offers distinct advantages. It is known for its excellent frequency stability resulting in very low phase noise. This is mainly caused by the feedback realization, consisting of two capacitors between base and emitter, C_1, and collector and emitter ,C_2, respectively, This arrangement effectively short-circuits the intrinsic noise sources and the low-quality intrinsic transistor reactances. At the same time, the collector-current conduction-angle can be reduced by choosing the ratio of the feedback capacitors properly. According to the LTV-theory [7] the current into the resonator should flow in narrow pulses at the maximum of the tank voltage, which is the case in well-designed Colpitts-type oscillators. This makes the Colpitts a very attractive to be used for a push-push type circuit.

The purpose of this paper is to demonstrate the advantageous features of combining push-push with Colpitts as well as using push-push with a static frequency divider. To our knowledge, this has not been published so far.

II. THE NEGATIVE RESISTANCE APPROACH

Regardless of the structure of the feedback network every oscillator can be designed applying the reflection-oscillator approach. For the classical Clapp oscillator, Fig. 1 shows the corresponding schematics with grounded collector. The HBT is reduced to the transconductance g_m for simplicity. In the following, the maximum negative input resistance is calculated for two cases:
1. $R_L = \infty$: R_L is not visible for f_0, e.g., in the push-push concept due to the location of R_L in a virtual ground node for the fundamental frequency (see Fig. 2).
2. $R_L > 0$, as is the case for fundamental single-ended oscillators.
These two cases are treated in detail in the following:

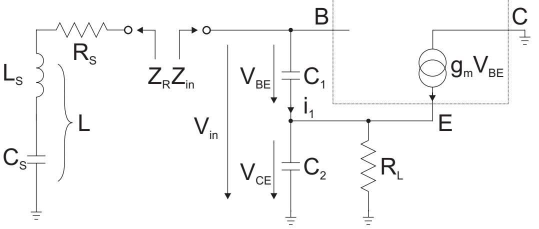

Fig. 1. Single ended Clapp oscillator with the transistor reduced to transconductance g_m

A. $R_L = \infty$

The input impedance is

$$Z_{in,1} = \underbrace{\frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}}_{imaginary} \underbrace{- \frac{g_m}{\omega^2 C_1 C_2}}_{real} \tag{1}$$

Thus, we have a frequency-dependent input impedance with negative real part, being a function of g_m and the feedback capacitors. As frequency increases C_1, C_2 need to be decreased in order to maintain a constant negative real part. In fact, however, g_m itself decreases with frequency, which further reduces the necessary capacitance values. The oscillation condition requires the negative real part to exceed the resonator losses, which are described by R_S:

$$R_S - \frac{g_m}{\omega_r^2 C_1 C_2} < 0 \tag{2}$$

The capacitive imaginary part is compensated to zero by a lumped inductor (Colpitts-configuration) or a series resonance circuit operating above its first resonant frequency (Clapp-configuration).

$$L = \frac{C_1 + C_2}{\omega_r^2 C_1 C_2} \tag{3}$$

As well known, a high loaded quality factor Q_L is of primary importance in minimizing phase noise. According to the Leeson-formula [1] one achieves a 6dB improvement in phase noise by doubling oscillator Q_L. A simple approximation for the loaded quality factor Q_L of the Clapp-configuration is given by [2]:

$$Q_L = \frac{1}{R_S}\sqrt{\frac{L_S}{C_S}} \tag{4}$$

Therefore, the ratio L_S/C_S must be maximized for highest Q_L but, since the losses R_S are mainly incorporated in the inductor, R_S follows L_S such that Q_L is limited by the inductor quality factor. Anyway, as frequency increases, $Re\{Z_{in,1}\}$ increases and is the true bottleneck for the maximum value of R_S thus limiting the maximum ratio L_S/C_S.

B. $R_L > 0$

Now we will consider the case of finite load resistance. The input impedance becomes

$$Z_{in,2} = \frac{1}{j\omega C_1} + \frac{R_L \frac{1}{j\omega C_2}}{R_L + \frac{1}{j\omega C_2}} + \frac{g_m R_L \frac{1}{j\omega C_2}}{j\omega C_1 \left(R_L + \frac{1}{j\omega C_2}\right)} \tag{5}$$

with the real part

$$Re\{Z_{in,2}\} = \frac{R_L\left(C_1 - C_2 g_m R_L\right)}{C_1 + C_1 C_2^2 \omega^2 R_L^2} \tag{6}$$

This means: By comparison we find $Re\{Z_{in,2}\} > Re\{Z_{in,1}\}$, i.e., the circuit with $R_L > 0$ provides less negative resistance than the one with $R_L = \infty$. Thus we can choose a much higher L_S/C_S-ratio in push-push oscillators than in their fundamental counterparts. Alternatively, to generate $Re\{Z_{in,2}\} = Re\{Z_{in,1}\}$ we can choose C_1 and C_2 larger in push-push oscillators and thus short-circuit transistor noise-sources more effectively. In both cases the push-push concept is superior in terms of phase noise.

III. APPLICATION OF THE PUSH-PUSH CONCEPT

In general, the push-push concept offers several advantages over single-ended designs:

- Since the transistors are operated at half of the desired output frequency, the usable frequency range of the devices can be extended, [6]
- Simultaneous generation of both the fundamental and second harmonic frequency is feasible [3]. Feeding f_0 into a frequency divider instead of $2f_0$ lowers the divider efforts (sec. V)
- Phase noise is reduced because of synchronization effects. [4],[5]
- High immunity against load-pull; because the second harmonic output is located at a virtual ground node, changes of the load affect the fundamental signal only indirectly.

Beyond this, the Colpitts oscillator in push-push configuration additionally offers:

- High output power at the second harmonic, fig. 5: The amount of harmonic content can be adjusted by C_1/C_2.
- Excellent phase noise properties, fig. 6, because transistor noise sources and low-Q elements are short-circuited.

IV. THE OSCILLATOR

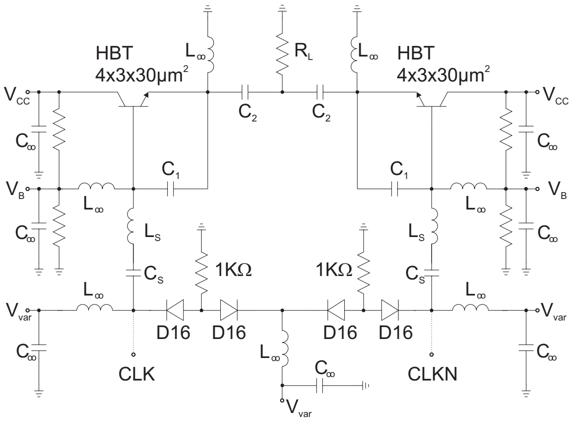

Fig. 2. Schematics of the X-band push-push Clapp oscillator. The second harmonic output is taken from the virtual ground plane.

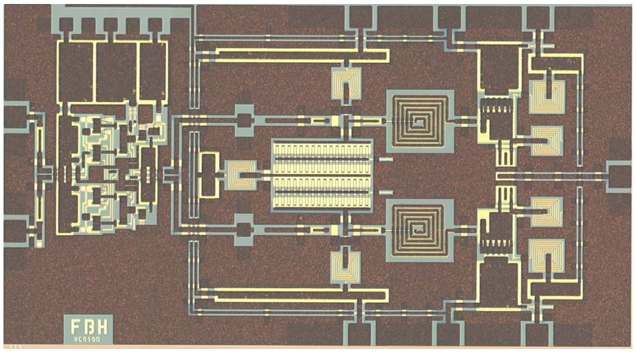

Fig. 3. Chipfoto of the X-band VCO together with integrated frequency divider. size: 2.8x1.5mm^2.

The circuits are realized fully monolithically as coplanar MMICs using the FBH 4” GaAs HBT process. The active elements are GaInP/GaAs HBTs with cut-off frequencies of $f_t = 45GHz$ and $f_{max} = 170GHz$, respectively. The epitaxial layers are grown by Metalorganic Vapor-Phase Epitaxy (MOVPE). Ledge technology is used to reduce 1/f noise. For further details see [8]. Fig. 2 shows the schematics of the oscillator core realized. The ciruit is based on the Clapp oscillator with the second harmonic output port placed at the common node of the feedback capacitors C_2. Circuit elements are chosen to obtain first-harmonic oscillation around $f_0 = 5GHz$. The fundamental signal across the varactors (CLK and CLKN in Fig. 2) is used to drive the frequency divider (Fig. 9). Although it is generally not recommended to additionally load the resonator in such a way this has been done for layout reasons. DC can be applied from one or both sides since the pads for V_{CC}, V_{Var} and V_{BE} are interconnected on chip. Current consumption at $V_{CC} = 3V$ is app. 145mA. V_{BE} is derived from V_{CC} using resistive dividers. Fig. 4 shows the output sprectrum when biasing the circuit from both sides - then the suppression of the odd harmonic content is better than 35dB. Having the DC applied from one side only the suppression reduces to 20dB. The fourth harmonic grows with V_{CC} and can be made as large as the second harmonic. In the case shown it is 14dB suppressed. To investigate the influence of the divider on the VCO behavior, additional versions were processed on the same wafer. The chip photo in Fig. 3) presents such a variation where the divider is disconnected to the VCO so that the oscillator can be measured separately. It turns out that the tuning range decreases by app. 50% when connecting the divider to the VCO, which is due to varactor loading. Redesigns are planned introducing an emitter follower between VCO and divider to decrease varactor loading. Two varactors are used in each half structure to avoid self rectification of the RF signal across the varactors, which always results in phase noise degradation. Fig. 7 presents the divider output signal measured by a spectrum analyzer when tuning the oscillator. Measurements were done single-ended with the other output terminated by 50Ω. Since the differential input signal for the divider at f_0 is half the output frequency at $2f_0$ one achieves in total a division by four. The measured output power is quite low at $V_{CC} = 3V$ but a strong function of V_{CC} and can be increased up to 0dBm when biasing the divider separately, see Fig. 11. The phase noise at the divider output is improved compared to the oscillator output by the value of 12dB, which is expected due to the frequency division by four. This documents that the phase-noise contributions of the divider are negligible.

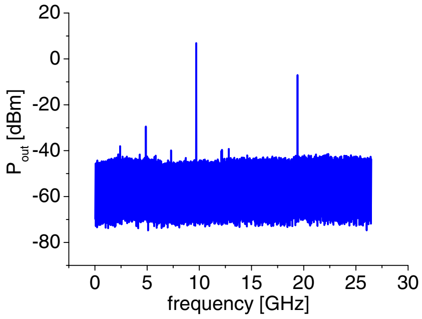

Fig. 4. output spectrum at second harmonic port with symmetric DC-supply ($V_{CC} = 3.0V$)

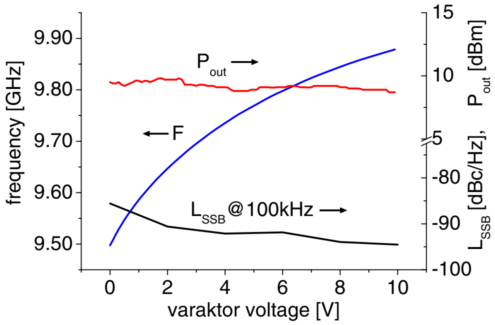

Fig. 5. Tuning characteristics at second harmonic port ($V_{CC} = 3.0V$)

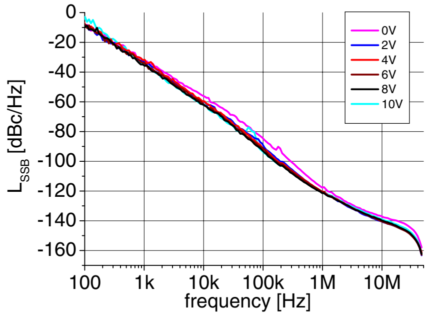

Fig. 6. L_{SSB} at second harmonic port ($V_{CC} = 3.0V$)

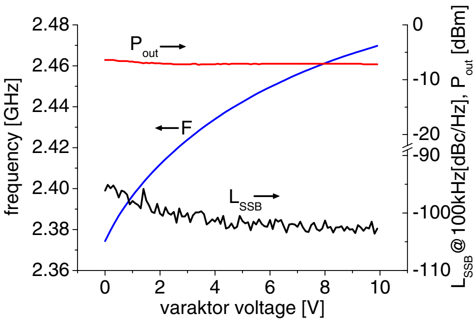

Fig. 7. Tuning characteristics and phase noise at the divider output ($V_{CC} = 3.0V$)

V. THE DIVIDER

The static frequency divider applies the well-known flip-flop approach and was realized also as a separate circuit for evaluation purposes. The measured data refers to unsymmetric operation with one input port capacitively grounded and one output port terminated by 50Ω and with *Bias1* and *Bias2* connected to V_{CC} in Fig. 9. DC current consumption depends on V_{CC} and grows linearly from 44mA at 3V to 140mA at 6V. The divider operates safely up to 7.5 GHz at input levels below -20dBm. Beyond this frequency, the power must be increased continuously. The maximum input frequency has been determined to be 10 GHz with an required input power of 0dBm. The ripple within the whole bandwidth is below 1dB. Varying the input level over 3 decades causes the output level to change by less than 3dB, fig. 10.

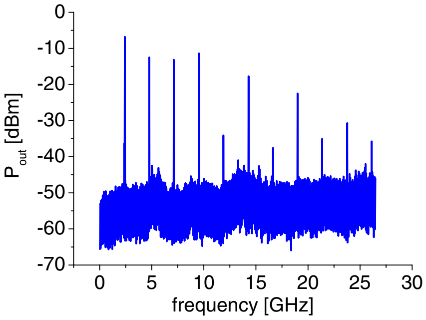

Fig. 8. output spectrum at divider port ($V_{CC} = 3.0V$, $V_{Var} = 0V$)

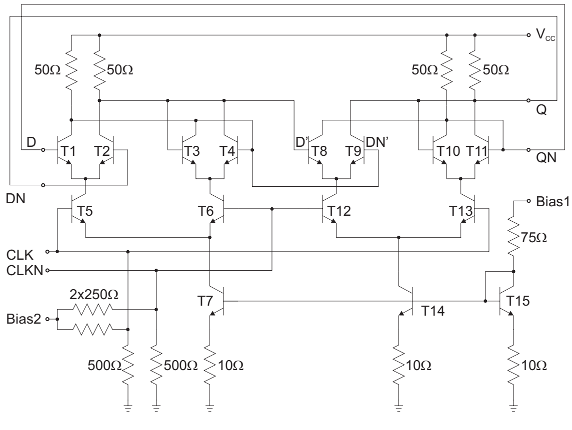

Fig. 9. Schematics of the divider.

VI. CONCLUSIONS

A novel circuit concept has been presented demonstrating an advantageous application of the push-push principle: Using it in conjunction with Colpitts oscillators yields potentially higher operational frequencies than achievable with fundamental Colpitts oscillators and leads to higher quality factors, since the load is not directly connected to the fundamental signal. Also, the approach preserves the inherent low-phase noise behaviour of Colpitts-type configurations. Additionally, the fundamental signal can be fed to a static frequency divider by two, which in total yields the frequency division factor by four at comparatively low efforts.

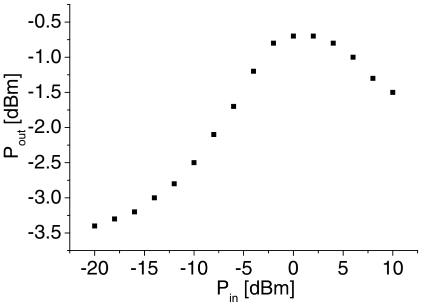

Fig. 10. Divider: P_{out} vs. P_{in} ($V_{CC} = 5V$, 5GHz).

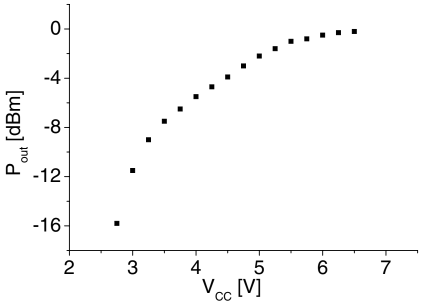

Fig. 11. Divider: P_{out} vs. bias voltage V_{CC} ($P_{in} = -10dBm$, 5GHz).

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