W-Band Flip-Chip VCO in Thin-Film Environment

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***Abstract* — A flip-chip packaging approach for W-band GaAs chips is presented using thin-film structures on silicon as carrier substrate. Reliability investigations indicate that, depending on bump size, the CTE mismatch is not critical and an underfiller does not provide distinctive benefits. A 77 GHz VCO GaAs-HBT MMIC is flip-chip-mounted to demonstrate validity of the packaging scheme.**

***Index Terms* — Thin film circuit packaging, Flip-chip devices, MMIC oscillators.**

I. MOTIVATION

Flip-chip mounting emerged as a promising packaging scheme for cost-effective module assembly in mm-wave systems. But there are still open questions regarding suitable carrier substrate to mount the chips on. The thin-film technology allows line systems which have small cross-sections adapted to the dimensions of the flip-chip interconnect and suitable for frequencies ranges above 80 GHz. Moreover, when using a thin-film microstrip line (TFMS) with shielding ground, the electrical properties of the carrier substrate do not influence the performance and can be used to attenuate unwanted substrate modes.

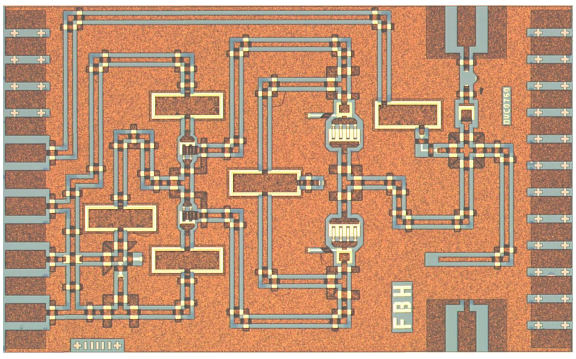

Fig. 1 Chip photo of the VCO MMIC. Chip size is (2.1 x 1.3) mm^2.

This paper reports on a process that combines flip-chip packaging with BCB thin-film structures on low-resistivity silicon (based on a BCB process carried out at the Fraunhoder IZM [1]) using thin-film microstrip transmission-lines and filter elements. As a demonstrator, single-function chips are mounted, in our case a VCO at 77 GHz. The MMIC is based on InGaP/GaAs HBTs, which combine low 1/f noise with relatively high transit frequencies.

This paper starts with a description of the VCO and then discusses two essential details of the flip-chip approach used, the bumping process and the underfiller topic. Finally, the experimental results obtained so far are presented. Some underfiller tests are currently in progress.

II. VCO TECHNOLOGY AND DESIGN

The VCO is an enhanced version of the circuit presented in [2]. It is fabricated on the FBH 4" MMIC process, which is based on InGaP/GaAs HBTs. The epitaxial layers for the HBTs are grown using Metalorganic Vapor-Phase Epitaxy (MOVPE). The frequency limits f_T and f_{max} for a standard one-finger device with (3 x 30) µm^2 emitter size are 50 GHz and 170 GHz, respectively. With the self-aligned base option even higher limit frequencies are obtained. To achieve low 1/f noise, a ledge technology is used to eliminate emitter-base surface-leakage.

Basically, the VCO consists of two reflection-type oscillators in a push-push configuration. The two identical circuits are coupled in a former ground node, where a virtual ground is formed. At this node the fundamental cancels out, but the second harmonic interferes constructively. Because of the virtual ground, the second harmonic can be extracted almost without influencing the fundamental.

Fig. 1 displays the chip photo. The symmetry line is horizontal in the middle of the circuit. The pads are enlarged in length, so it is possible to measure the chip on-wafer after the bumps are processed. Several alignment marks are provided. At the right and the bottom side of the chip there are several unused pads, which can be connected optionally to improve mechanical stability.

III. Bump Technology

Au/Sn solder bumps are especially suited for flip-chip assembly of optoelectronic and RF devices. The manufacturing process of GaAs microwave chips already includes Au plating, which makes the use of electroplated Au/Sn bumps attractive. The bumps are manufactured by electroplating gold and tin in subsequent process steps. After the plating process the bumps consist of a thick gold layer and a thinner Sn layer on top. When the bumps are heated up to above 280 °C a solder cap forms, which consists of the gold-rich eutectic microstructure with the composition of 80 wt.-% Au and 20 wt.-% Sn. After this process step, the so-called bump reflow, the bumps consist of a Au layer with an eutectic solder cap on top.

In a cross-sectional view, the Au layer appears like a socket. It is separated from the eutectic solder cap by a layer of the intermetallic Au_5Sn-phase, which is referred to as ζ-phase in the following. The ratio of gold and tin has to be chosen such that, after reflow, a gold layer is left below the eutectic cap and the layer of ζ-phase. This prevents the liquid eutectic solder from getting in direct contact with the plating base. The remaining Au acts as a compliance layer thus enhancing reliability. During flip-chip assembly only the eutectic part melts while the rest of the bump remains solid [3, 4, 5].

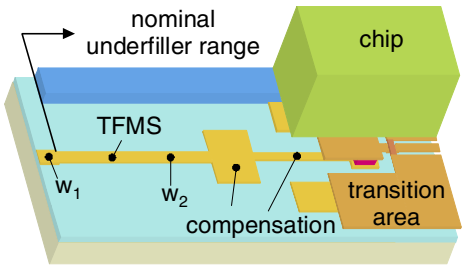

Fig. 3 Flip-chip mount with underfiller

The Au/Sn-bumps are plated on top of a 3 µm thick Au layer. As the substrate pads are made of 6 µm thick Au, the molten eutectic solves Au so that the composition of the liquid gets Au-richer until the composition of the ζ-phase is reached. As a consequence, the flip-chip solder joints consist of Au on the chip side, a region of ζ-phase and a Au layer on the carrier-substrate side. The eutectic microstructure is not visible any more (see Fig. 6).

IV. Application of Underfiller

In a first step, the interconnect was optimized for minimum reflection in the 77 GHz range [6] for the structure without using an underfiller. Using GaAs chips in conjunction with a Si-based thin-film substrate (15 µm thickness), however, the CTE mismatch needs to be accounted for. This is the motivation why an underfiller is applied, which is to lower mechanical shear forces on the bumps connecting carrier and chip.

The underfiller is dispensed between chip and substrate but will also cover part of the surrounding structures on the carrier substrate (see Fig. 3). Hence, in a second step, the influence of the underfiller was included also in the design. Fig. 3 depicts the transition and the TFMS compensation elements as well as the 50 Ω line systems in both, free space (MS width w_1) and underfiller range (MS width w_2).

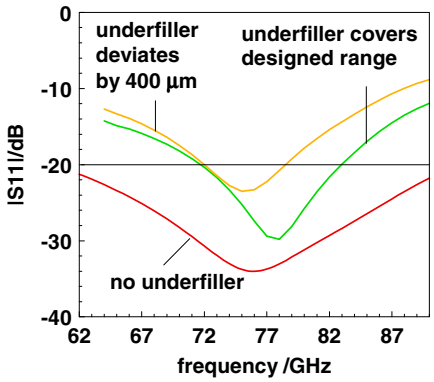

Fig. 4 Reflection coefficient of the interconnect without and with underfiller (see Fig. 3) including both its nominal extension and a deviation by 400 µm.

Unfortunately, the underfiller has a dielectric constant in the range of ε_r=3...4 and can disturb electrical properties of the circuits and the line structures on the substrate.

Hence, the relevant elements had to be re-optimized. The interconnect behavior was improved by adding proper compensation structures on the carrier substrate (while the in-out cell on the chips is fixed in order to save on expensive chip area).

When dispensing the underfiller it comes to capillary flow and spreading. This means that the underfiller covers also a certain portion of the connecting lines and compensation structures on the carrier substrate around the chip. Two issues are important to be considered:

1. The underfiller must cover the compensation structure completely. If it is covered only partially, the structure is detuned. Since the compensation is sensitive to parameter variations, the result is probably worse than without any compensation. In our case, the compensation structure is located close to the transition in order to be certainly covered entirely.

2. The spreading range of the underfiller must be confined as good as possible, with regard to both lateral range and height.

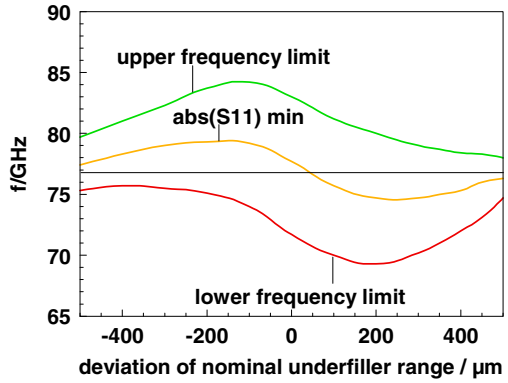

Fig. 5 Bandwidth and frequency with minimum of $|S_{11}|$ versus underfiller extension (deviation from the nominal underfiller range).

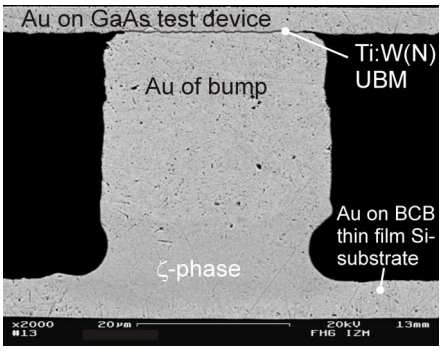

Fig. 6 Cross-sectional SEM image of a flip-chip bump interconnect after assembly.

It is obviously that the flow and thus the final extension of the underfiller cannot be restricted to a clearly defined range. A certain deviation of the dimensions intended must be taken into account and the interconnect must be designed to meet the specs within these tolerances. In Fig. 4, the reflection coefficient is plotted as a function of frequency for a transition with and without underfiller. In order to demonstrate the influence of actual coverage by underfiller, the nominal length extension of 800 µm as well as a deviation of 400 µm off the nominal length is considered.

This nominal length of 800 µm was chosen in order to meet all technological and electrical requirements, i.e., the underfiller must cover the compensation area entirely, and one must consider the dispensing process itself, which needs some space for the tools.

From the curves in Fig. 4 we can conclude that this interconnect, together with the underfiller process, is feasible as long as the underfiller extension deviates less than 400 µm from the nominal value. Fig. 5 illustrates this in more detail showing the upper and lower limit of the bandwidth, where the reflection coefficient remains below -20 dB. As can be expected, the useful bandwidth shrinks with growing deviation of the underfiller extension from its nominal value. Up to a deviation of 400 µm, however, return loss exceeds 20 dB in a sufficiently broad band.

V. Experimental Results

The bumps are deposited on the GaAs-wafer. After dicing the VCOs were measured a first time to ensure known-good dies. The qualified chips are then assembled on the silicon thin-film substrates and reflow-soldered. Fig. 6 presents a cross-sectional SEM image of a flip-chip bump interconnect. Fig. 7 shows a top view of the flip-chip mounted VCO.

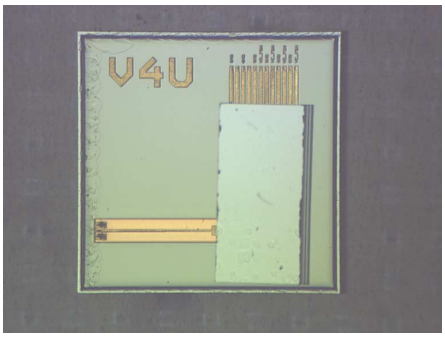

Fig. 7 The flip-chip mounted VCO (top: bias feeding; left side : RF output port).

The microwave measurements are plotted in Figs. 8 and 9. Fig. 8 presents the tuning curve of three oscillators before and after the flip-chip assembly. One observes only a slight frequency detuning due to mounting, which is smaller than 250 MHz (< 0.3 %). This is below the temperature drift of the circuit.

Fig. 9 shows the measured output power of the three VCOs before and after assembly. The ripple on the curves is attributed to the measurement set-up and is related to the line length between DUT and power-sensor. It is observed for both cases - before and after the assembly. The measured output power after flip-chip assembly deviates by less than 2 dB. For one of the oscillators almost the same power is measured after the assembly. It can be stated that the power degradation is in the range of the measurement accuracy.

In order to assess the problems related to the CTE mismatch between the GaAs chips and the Si-based thin-film substrate, an extensive reliability study was carried out.

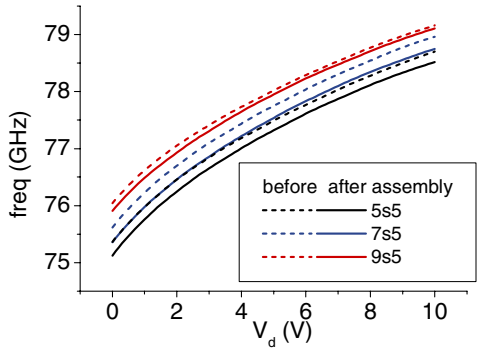

Fig. 8 Tuning characteristics of 3 VCO samples before and after the flip-chip assembly (frequency against varactor voltage).

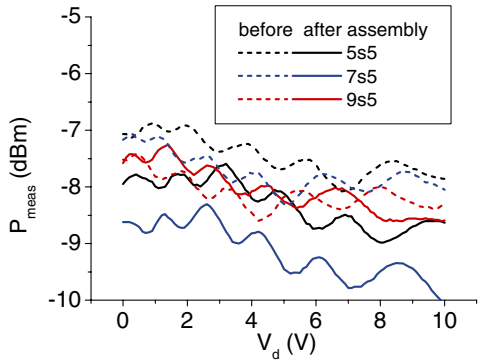

Fig. 9 Measured output power of 3 VCOs samples as a function of varactor voltage V_d.

For this purpose, 3.5 mm square GaAs test chips were used, AuSn reflow-soldered on Si thin-film substrates. Two different bump sizes of 30 and 50 µm diameter were investigated and underfilled and non-underfilled samples were tested during temperature cycling between -55 and +125°C. Assemblies using 30 µm bumps failed significantly earlier than the versions with 50 µm bumps (for details see [4]). On the other hand, an essential improvement in reliability cycles by using an underfiller could not be seen. This is an interesting finding because it contradicts the common believe that underfiller is preferable because of improved reliability.

Though the differences between the underfilled and non-underfilled version are not significant, all samples survived thermal cycles in the range from 1250 to1650. These values clearly indicate a reliable connection between chip and carrier substrate for both cases. For realistic chip sizes in the order of 1 mm² (rather than 3.5 x 3.5 mm² for the test chip) situation should improve further.

VI. Conclusions

A flip-chip packaging scheme for W-band modules is presented using a low-resistivity Si substrate with BCB thin-film microstrip transmission lines as the carrier. A GaAs VCO MMIC was mounted and measured with good results: Only small degradation in resonance frequency (below 0.3 %) and output power (less than 2 dBm) are observed. Reliability investigations on test samples indicate that – despite the CTE mismatch between GaAs and Si - underfilling is not necessary because it does not improve reliability considerably. Rather, one should pay attention to keep bump size large enough (50 µm in our case). The performance of the 77 GHz VCO demonstrates suitability of this approach as a relatively low-cost and high performance assembly technique.

Acknowledgements

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