A 40 Gbps GaAs-HBT Distributed Amplifier with an Over-f_T Cut-Off Frequency: Analytical and Experimental Study

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Abstract — **The bandwidth potential of HBT distributed amplifiers following the traveling-wave concept (TWA) is studied. Basic parameters are the transistor characteristics as well as the losses of the artificial transmission lines. As a result, a relation between f_T and f_{max} of the HBTs and the –3dB cut-off frequency of the amplifier is derived. Based on this, an over-f_T cut-off-frequency TWA is realized with 6 dB broadband gain and 42 GHz f_c using GaAs HBTs with 36 GHz f_T and 170 f_{max}.**

Index Terms — **Distributed amplifier, GaAs, HBT, f_T, f_{max}.**

I. INTRODUCTION

In the framework of the optical fiber transmission systems, the rapid development of multimedia communication has raised the demand for high-speed transmission circuits and systems. Several ultra high-speed amplifiers using high-performance technologies such as InP HEMTs or HBTs [1], or GaAs pHEMTs [2] have been realized. But such high-end processes are expensive and, therefore, the new target today is to explore the high-bit rate capabilities of technologies with lower cost. Thus, interesting results using CMOS have already been reported [3] as well as 40 Gbps chips realized in SiGe-HBT technology [4]. Despite their high cut-off frequencies, however, the Si technologies still suffer from important frequency limitations when driving large currents, restricting them to low output-voltage swings. Some other examples have also been realized with GaAs HBT [5] and have shown interesting results in terms of output voltage swing at 40 Gbps, but only when using Bessel-like gain characteristics in order to compensate for the relatively low cut-off frequencies.

The objective of this work is to derive a guideline how to predict the maximum –3dB cut-off frequency one can achieve with a given technology. Our study focuses particularly on GaAs-HBT based amplifiers, however, it can be applied also for other HBT technologies if the right approximations are taken into account. The theoretical results are backed by experimental results using the FBH GaAs-HBT MMIC process.

The paper is organized as follows: After a brief description of the process and modeling tools, Sec. III presents the circuit design considerations, while Sec. IV provides the experimental results.

II. TECHNOLOGY AND TRANSISTOR MODEL

In this section, the technology used and the transistor CAD model are described briefly. The HBT MMICs are fabricated on the FBH 4" process line. The epitaxial layers are grown by Metalorganic Vapor-Phase Epitaxy (MOVPE). For further details see [6].

Excessively high f_{max} values (beyond 170 GHz at V_{CE} =3 V) are achieved as compared to the more industry-standard f_T values (36 GHz at V_{CE} =3 V). While f_T is mainly determined by the layer structure, f_{max} can be increased by optimizing the process. In our case, mainly base resistance R_B and base-collector capacitance C_{bc} are modified. R_B is reduced by smaller under-etching of the emitter metal, which minimizes spacing between emitter and base metalization. In order to reduce the extrinsic base-collector capacitance $C_{bc\text{-}ex}$, we apply an additional He^+-implantation in the outer region of the base fingers. Together with a reduction of the base-emitter distance from 1.3 µm to 0.5 µm, these process optimizations increased f_{max} from 95 GHz to 170 GHz.

A customized CAD library containing both passive and active devices is used for circuit simulation. Key part is the FBH HBT model [7]-[8]. It includes partition of intrinsic and extrinsic base-collector diode, non-ideal base currents, self-heating, base-emitter and base-collector break-down, current-dependence of base-collector capacitance $C_{bc,intr}$, and collector transit time τ_c (i.e., velocity modulation and Kirk effect, which are responsible for the f_T and f_{max} peaking to be seen in Fig. 1).

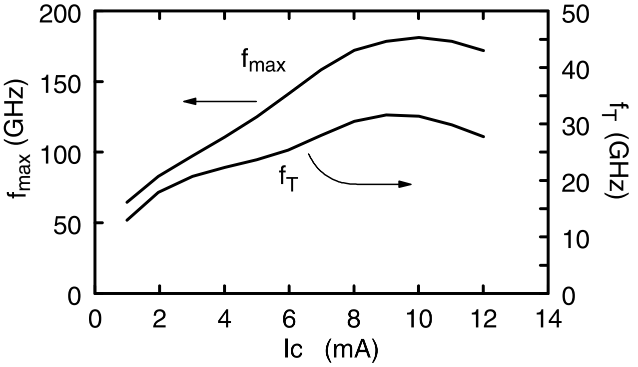

Fig. 1. Extracted values of f_T and f_{max} against collector current for a 2x10 µm² HBT at V_{CE}=3 V.

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III. CIRCUIT DESIGN

A. Distributed gain

According to the principle of distributed amplification, a wave-wave amplifier (TWA) is formed by the parallel connection of amplifying cells via inductors. Input and output capacitances of the active devices together with the inductances and connecting lines form equivalent transmission lines. These artificial input and output lines are designed to have, in principal, 50 ohms characteristic impedance and to achieve equal and flat group delay over the band.

Thus, an HBT-based TWA can be represented by the equivalent circuit in Fig. 2.

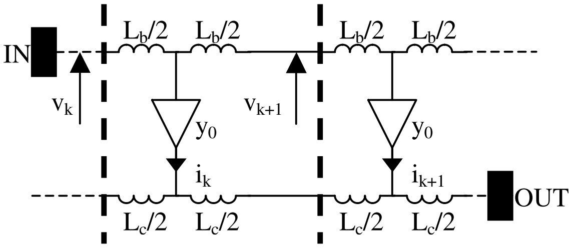

Fig. 2. Distributed amplifier representation.

L_b and L_c describe the added inductances to form the input and output artificial transmissions lines, respectively, v_k is the signal voltage swing at the reference plane of each inductor cell, i_k the generated current for each cell, and $y_0 = i_k/v_k$ the transconductance gain.

The collector (output) line is terminated by a 50 ohms load as is the base (input) line. Thus, the backward waves are absorbed in the 50 Ohm resistor, which also feeds the base and collector bias of the transistors. In order to identify and understand the effect of the intrinsic transistor elements on cut-off frequency, one must simplify the circuit properly. Therefore, we assume that the ends of the artificial transmission lines are matched and that the group-delay is equal for both lines. Then, the voltage gain of the distributed amplifier can be written as follows:

$$G_v = \frac{1}{2} \cdot Z_{load} \cdot y_0 \cdot \sum_{k=0...(N-1)} e^{-k(\gamma_b+\gamma_c)+(N-1)\gamma_c} \qquad (1)$$

where Z_{load} is the impedance at the output, and the factor 1/2 is a mean value depending on the real matching conditions, which reflects the fact that the current wave on the collector line flows in both directions, so that only half of it is collected at the load. The terms in the sum correspond to the transmission line losses, which, in our case, are low (below 0.5 dB at 40 GHz for 10 cells and thus negligible compared to the term y_0, which is mainly responsible for the 3dB cut-off frequency). N denotes the number of cells. In addition to this, and to stay on the safe side of this approximation, we will use a small number of cells. Thus, overall gain and cut-off frequency will be considered to depend mainly on the cell gain.

B. Cell transconductance

The chosen gain cell is a cascode pair. This provides wide bandwidth and good isolation by canceling the Miller effect (the bridge capacitance becomes smaller than in the case of a simple common emitter). In addition, a feedback resistor on the emitter is used to broaden the bandwidth and to increase the input impedance of the cell. Therefore, by ignoring the base-collector cascade capacitance, the small signal equivalent circuit can be approximated as depicted in Fig. 3.

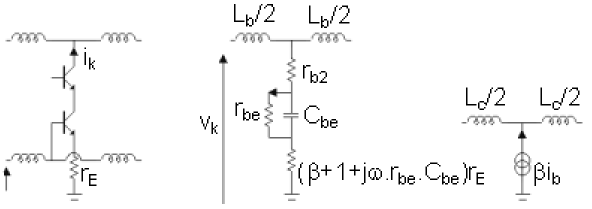

Fig. 3. Small-signal cascode cell equivalent circuit.

C_{be} contains the capacitance at the input as well as the transit time on the base. The resistance r_E is multiplied by a factor depending on β, C_{be} and r_{be} to take into account the modification of the input impedance of the transistor due to the feedback resistor.

Then, the cell transconductance $y_0=i_b/V_k$ can be calculated as :

$$|y_0| = \frac{\beta}{\sqrt{\left[R - \frac{\omega^2 \cdot L_b}{2\omega_g}\right]^2 + \omega^2\left[\frac{L_b}{2} + \frac{1}{\omega_g}(r_E + r_{be})\right]^2}} \qquad (2)$$

with $R = r_{b2}+r_{be}+(\beta+1)r_E$, and $\omega_g = 1/C_{be}L_b$. The operating bias point is chosen as a trade-off between high values of f_T and f_{max}. In our case, the small-signal V_{ce} bias is set to approximately 3 V, with I_c=10 mA. At this operating point, the equivalent circuit elements are:

R_{b2}	r_{be}	C_{be}	β	C_{bc} (int + ext)
8,3 Ω	601 Ω	0,68 pF	103	18 fF

r_E is responsible for broadening the band with the feedback effect on the emitter but also for the increase of the input impedance $(\beta+1+j\omega C_{be}r_{be})\ r_E$, which lowers the value of the inductor, required to reach 50 Ω characteristic impedance of the artificial transmission line. As a consequence, the cut-off frequency of the amplifier is increased. At the same time, r_E decreases the value of the gain, and the maximum value of r_E is limited by the DC gain. For a minimum of 6 dB broadband gain and a number of cells between 4 and 6, which ensures to have negligible transmission-line losses, one has for the voltage gain with eqns. (1) and:

$$\left|G_v\right|_{\omega=0} = 5 \cdot \frac{1}{2} \cdot Z_{load} \cdot \frac{\beta}{r_{be} + r_{b2} + (\beta + 1)\, r_E\,(max)} = 2$$

Thus, for a 50 Ω load and an absorption resistor at the end of the collector line between 40 and 50 Ω, we find r_E values between 25 and 35 Ω . We will use the smallest value for the following steps, so that the lowest value of the maximum f_c will be calculated.

C. The –3dB cut-off frequency

The –3dB cut-off frequency f_c or ω_c is defined as:

$$\left|y_0\right|_{\omega=wc} = \frac{1}{\sqrt{2}} \cdot \left|y_0\right|_{\omega=0}$$

From the expression for the transconductance gain of the amplifying cell, we can calculate the cut-off frequency:

$$f_c = \frac{1}{2} \cdot w_g \cdot \sqrt{\frac{2}{L_b^2} \cdot \left[\sqrt{B^2 + \frac{R^2 \cdot L_b^2}{\omega_g}} - B\right]} \qquad (3)$$

with $B = \frac{L_b^2}{4} + \left[\frac{r_e + r_{be}}{\omega_g}\right] - \frac{R \cdot L_b}{\omega_g}$

and knowing that $f_T \approx \frac{1}{2\pi} \cdot \frac{1}{\frac{r_{be} \cdot C_{be}}{\beta + 1}}$

and $f_{max} \approx \sqrt{\frac{f_T}{8\pi\, r_{b2}\, C_{bc-int}}}$

We can then plot f_c as a function of f_{max} for a fixed value of f_T. For the FBH process, the highest value provided for this type of transistor is f_T~36 GHz (see Fig. 1.)

From Fig. 4 one can see that assuming L_b values between 200 and 400 pH cut-off frequency is higher than the transit frequency of the transistor provided that f_{max} is high enough. In our case, f_{max} is around 170 GHz. This means that a maximum cut-off frequency of 45 GHz can be expected, with a transit frequency of 36 GHz and for an inductance of the base line of 300 pH, which is an interesting value for the impedance matching of the artificial transmission lines.

C. Circuit optimization

The problem of the gain-frequency slope is mainly solved by the unit-cell design. On the one hand, by optimizing numerically the value of the emitter feedback resistor. A 25 Ω resistor was used to flatten the gain over the bandwidth.

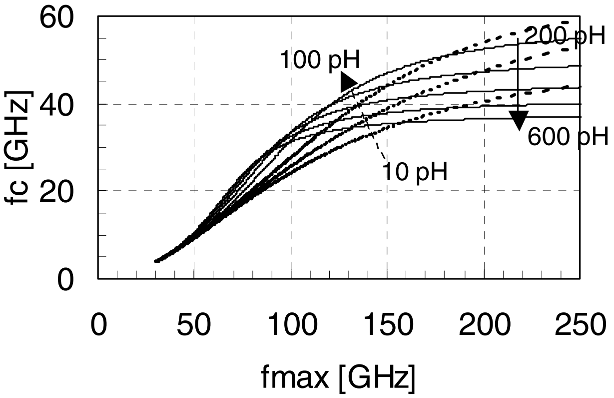

Fig. 4. -3 dB f_c versus f_{max} for a constant f_T = 36 GHz and different values of L_b.

On the other hand, the decoupling of the second cascode base represents a key condition for high-frequency operation. In our design, the base is locally decoupled with a series dump resistor of a few ohms and 5 pF capacitor to the nearest emitter and connected to a longer DC bias line. Thus, floating ground planes due to the dimensions of the circuit will not influence the performances of the amplifier. However, this node was carefully simulated because it can cause the real part of the output impedance to become negative, which, in consequence, can lead to instabilities if it is too sharply decoupled. By means of supplementary resistors added on the artificial transmission lines and the feedback resistor on the emitter, a smooth decreasing slope gain is achieved.

A second problem, the gain ripple, was solved by carefully optimizing the coplanar transmission lines for good matching while maintaining a low variation of the group delay and a smooth decrease of S_{21} at high frequencies. Fig. 4 presents the chip photo. Because input and output parasitic capacitances of the transistors may differ, equalizing the group delay can require input and output lines to have different lengths.

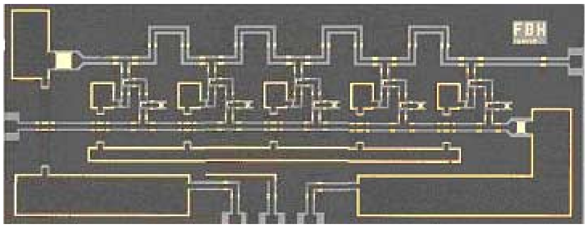

Fig. 4. Chip photo.

The collector line is terminated by a 40 ohms load, which is designed to provide DC bias power without significant thermal effects. The backward waves on the input transmission line are absorbed in a 30 ohms resistor, which also feeds the base bias of the transistors. The ground areas are interconnected along the transmission lines and around discontinuities to suppress parasitic modes and to ensure correct ground-current paths.

IV. MEASUREMENTS

On-wafer small signal measurements reveal 6 dB broadband flat gain with a 3 dB cut-off-frequency of 42 GHz.

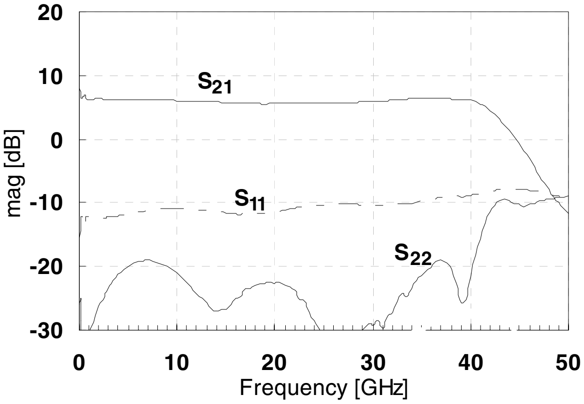

Fig. 5. Measured S parameters of the TWA.

DC consumption of the circuit is about 280 mW for a 46 mA DC current and about 6 V collector voltage. Input and output matching is better than -5 dB within the bandwidth. Under the measurement bias conditions, transit frequency f_T of the transistor was 36 GHz. (see S-parameters measurements in Fig. 3). The f_c-to f_T-ratio is of about 1.2 and thus larger than unity. This is an interesting result, which is attributed to the high f_{max} to f_T ratio. It is very useful in pushing the frequency limits of distributed amplifiers.

IV. CONCLUSIONS

The design of broadband amplifiers is investigated with the aim to predict maximum TWA cut-off frequency as a function of the transistor frequency limits. A small-signal analytical description for the circuit gain is derived, as a function of the small signal parameters of the transistor equivalent circuit, the feedback resistor, and the artificial transmission lines. The final expression provides a quite reliable value for the maximum -3dB cut-off frequency, given a realistic range for f_T and f_{max}. Typically, with an f_T around 36 GHz and f_{max} of 170 GHz, one can achieve a cut-off frequency around 45 GHz if the number of stages is low enough so that transmission line losses can be neglected.

On the one hand, this first result confirms the common empirical observation that f_c depends more on f_{max} than on f_T for distributed amplifiers. On the other hand, it provides an analytical tool allowing for the prediction of f_c, based on the general frequency characteristics of the transistor. For the specific transistor parameters used here, for instance, it turns out that f_c grows stronger with f_{max} than with f_T, and can achieve higher f_c than f_T but reaches saturation when increasing f_{max} further. Thus, an optimum f_{max}/f_T ratio exists.

Based on this result, a TWA circuit was optimized further by means of CAD software and realized as an MMIC. It shows a relatively high –3dB cut-off frequency of 42 GHz and a broadband gain of 6 dB, for a transition frequency of the transistors of 36 GHz. This is an interesting result important for understanding the operation of distributed amplifier for high bit rate transmission systems.

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