

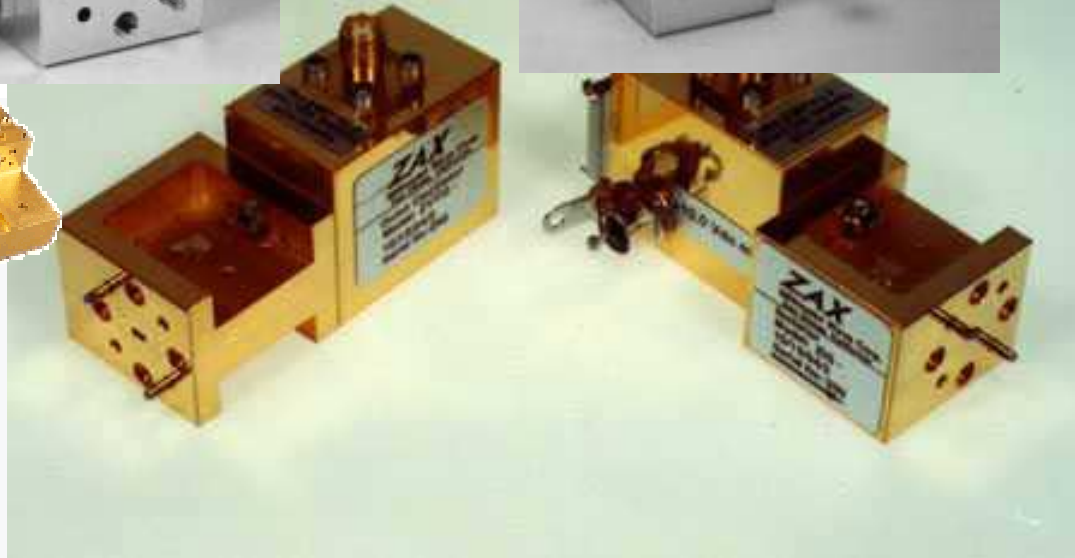
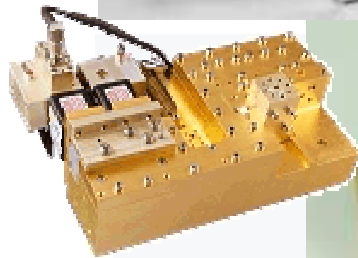
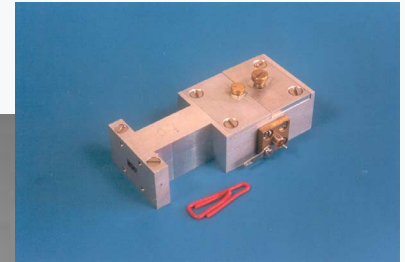
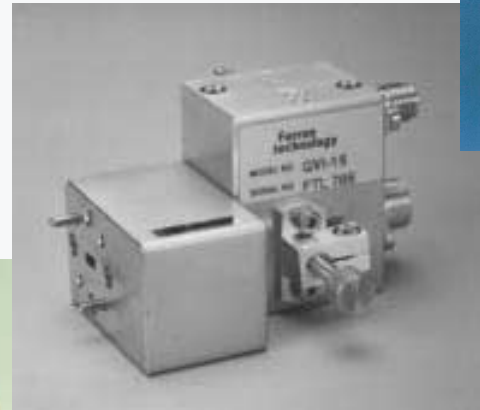
# Recent Advances in Low-Noise Monolithic Signal Generation Techniques Above 10 GHz

**F. Lenk and W. Heinrich**

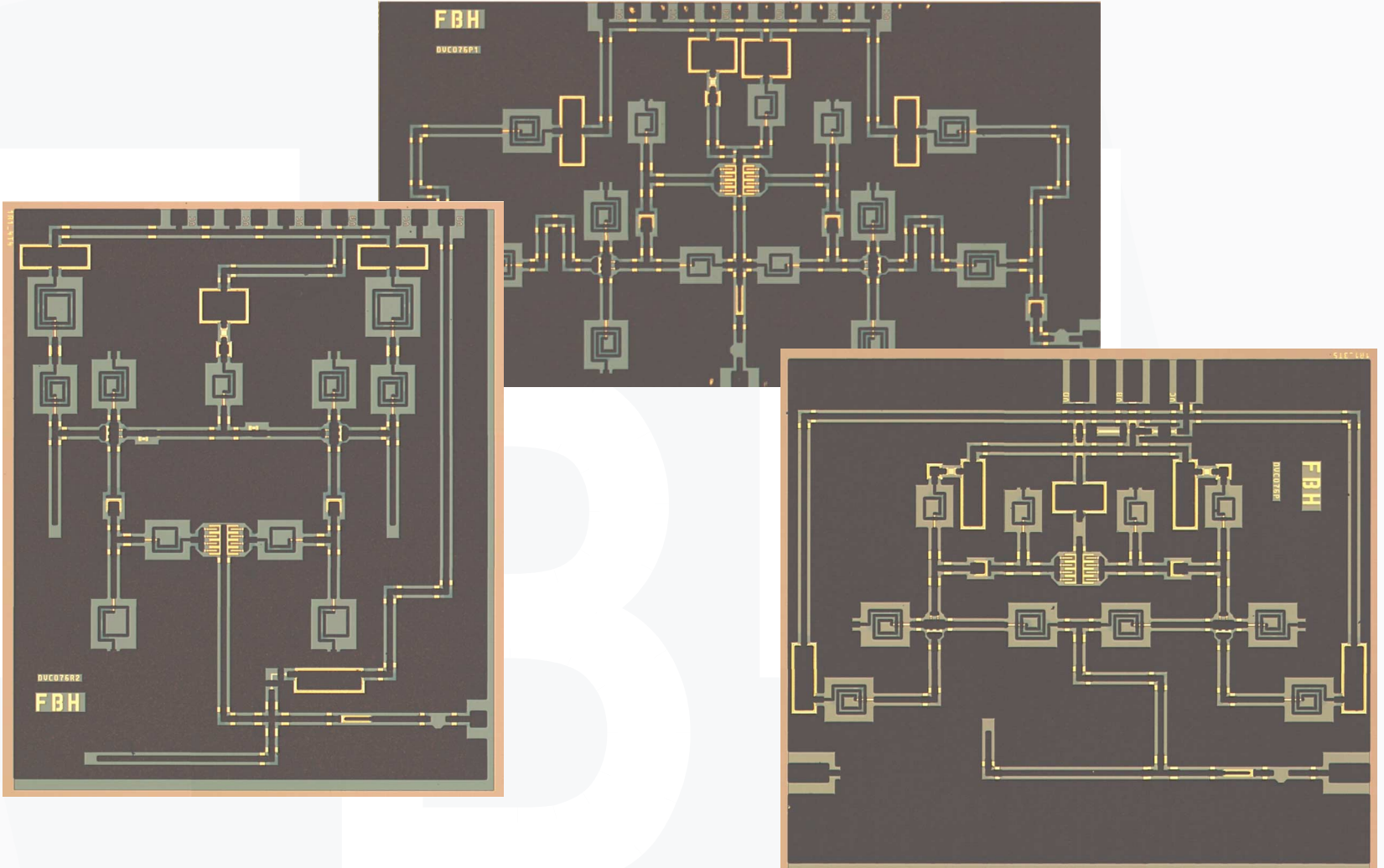
with contributions by M. Schott,  
P. Heymann, J. Hilsenbeck, P. Kurpas

**Ferdinand Braun Institut (FBH), Berlin**

# The clean mm-wave source: How it looks like



# ... and how it should look like



## The ideal mm-wave source:

- low phase-noise
- fully monolithic (MMIC)
  - cheap / small
- enough output power
- interface to PLL @ low frequency

How to realize low phase-noise

MMIC oscillators?

# This talk: on low-noise VCO

- not on phase-noise simulation,  
...but on **design strategies**
- not on “low” frequency oscillators,  
...but on devices operated at their **frequency limits**
- not on assembly techniques,  
...but on **fully monolithic circuits** with integrated resonator
- not on locking,  
...but on **free-running** oscillator performance

# Specific constraints

- **fully monolithic circuits**
  - low Q-values
  - restricted element ranges
- **devices operated at their frequency limits**
  - accuracy of models becomes worse
  - simplifications difficult
  - reduced gain / increased parasitics
  - design strategies / possibilities restricted

# Outline

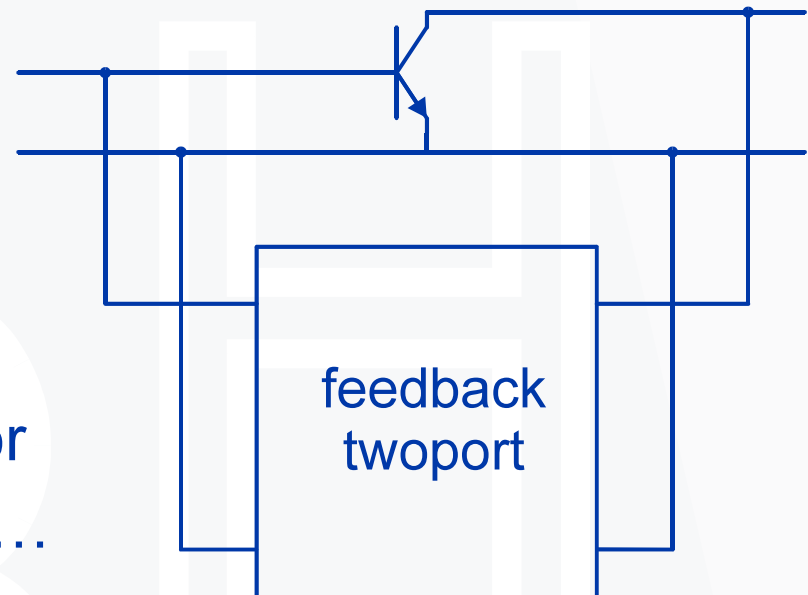
- **high frequency fundamentals**
  - concepts: Colpitts, classical  $\mu$ wave, ...
  - loaded  $Q_L$  calculation, bias dependence
  - push-push
  - misc: load-pull effects, phase-noise simulation
- **recent advances**
  - published examples
  - commercial MMIC

# Oscillator principle

- in-phase feedback of an active device

- kind of feedback structure classifies oscillator type:

- $\pi$  – type: LC oscillator  
e.g. Colpitts, Clapp, ...
- T-type: classical  $\mu$ wave reflection type



# Oscillator principle

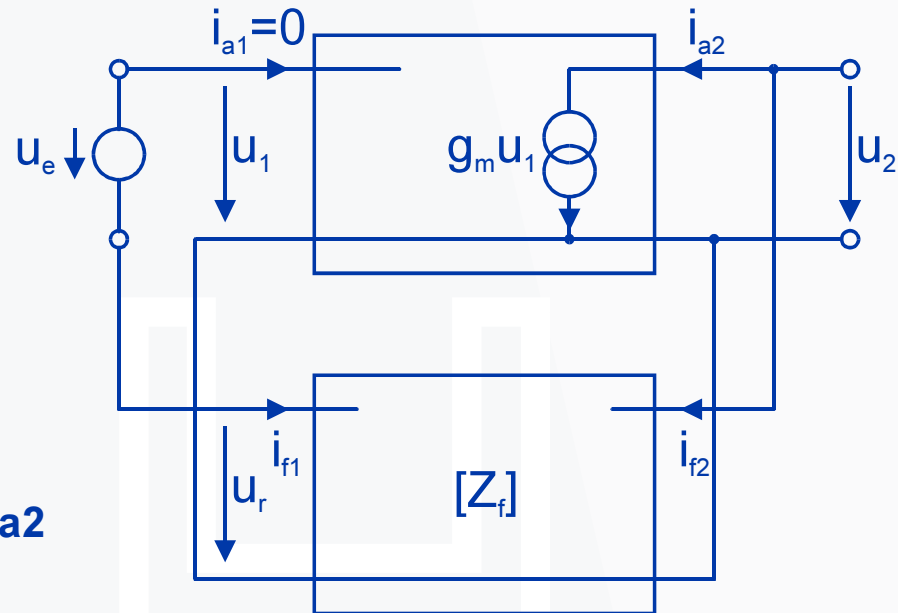
- textbook derivation

$$i_{a2} = g_m (u_e + u_r)$$

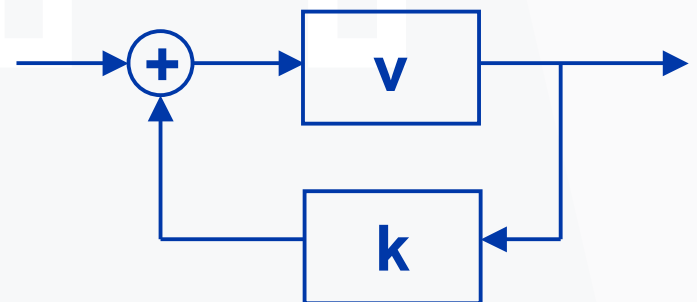
$$u_r = Z_{f11} i_{f1} + Z_{f12} i_{f2} = -Z_{f12} i_{a2}$$

- effective transconductance  $g'_m$

$$g'_m = \frac{i_{a2}}{u_e} = \frac{g_m}{1 + Z_{f12} g_m} \hat{=} \frac{v}{1 - k v}$$



... analog control theory



# Oscillator terms

- “characteristic equation”

$$1 + Z_{f12} g_m$$

- loop gain (dimensionless)

$$S_v = Z_{f12} g_m$$

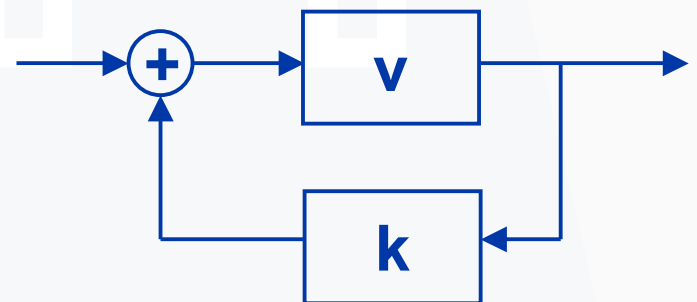
- oscillation condition

$$S_v = |S_v| e^{j\varphi}, |S_v| > 1, \varphi = \pi$$

- loaded  $Q_L$

$$Q_L = \frac{\omega}{2} \left| \frac{d\varphi}{d\omega} \right|, \omega \rightarrow \omega_0$$

$$\frac{g_m}{1 + Z_{f12} g_m} \hat{=} \frac{v}{1 - k v}$$



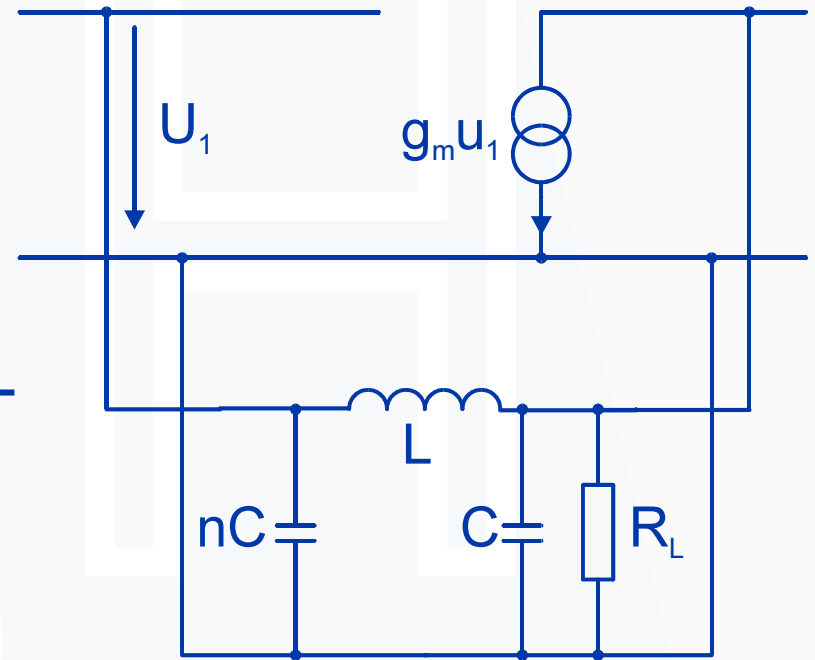
# Well known: Colpitts oscillator

- oscillation condition

$$\omega_0^2 = \frac{n+1}{n L C}$$

- loaded  $Q_L$

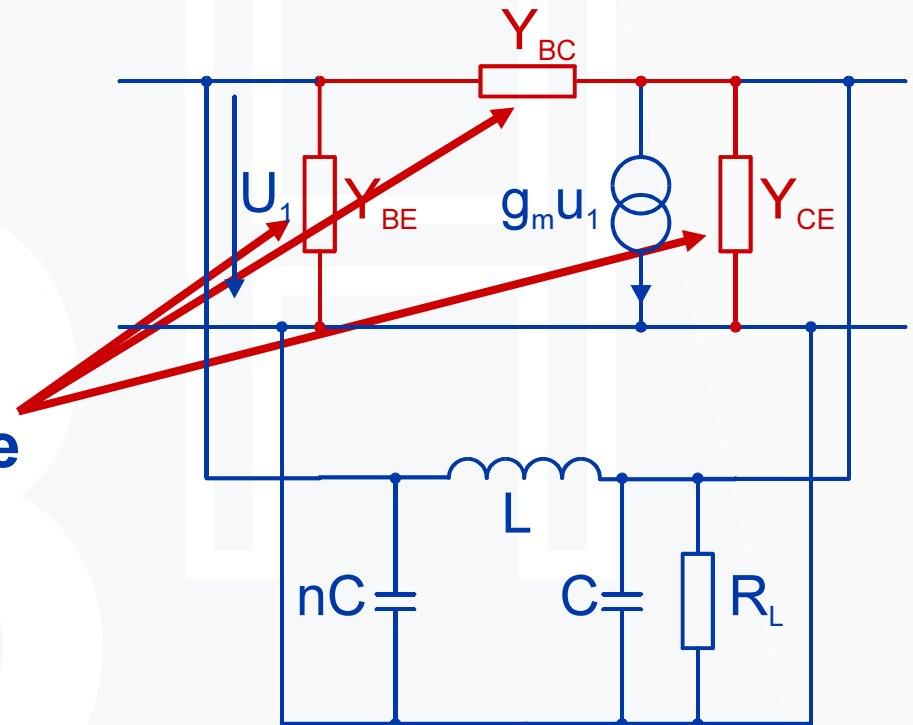
$$Q_L \approx R_L \left( \frac{n+1}{n} \right)^2 \sqrt{C/L}$$



# Problems for higher frequencies

- (general) transistor cannot be approximated by an ideal current source

not negligible

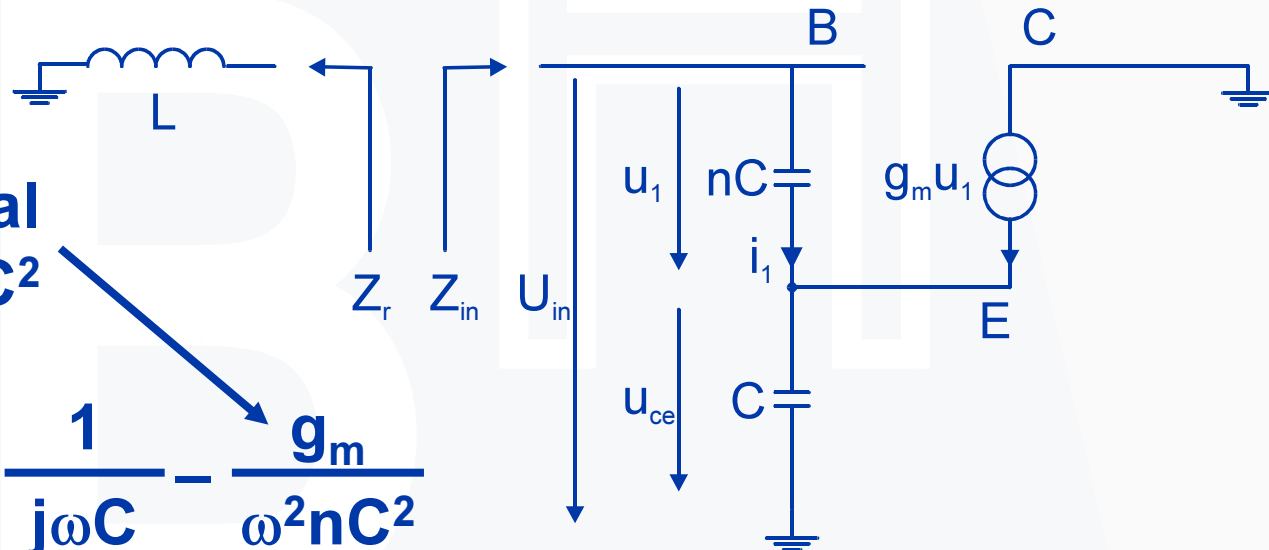


# Problems for higher frequencies

- (general) transistor cannot be approximated by an ideal current source
- (Colpitts) capacitances for reasonable  $R_{in}$  become too small

negative real  
part  $R_{in} \propto 1/C^2$

$$Z_{in} = \frac{1}{j\omega nC} + \frac{1}{j\omega C} - \frac{g_m}{\omega^2 nC^2}$$



# Problems for higher frequencies: Possible solutions

- **use another oscillator topology**
  - e.g.: reflection-type oscillator better suited for low gain / high frequency
- **include parasitics in design**
- **design @  $f_{osc}/2$** 
  - push-push principle

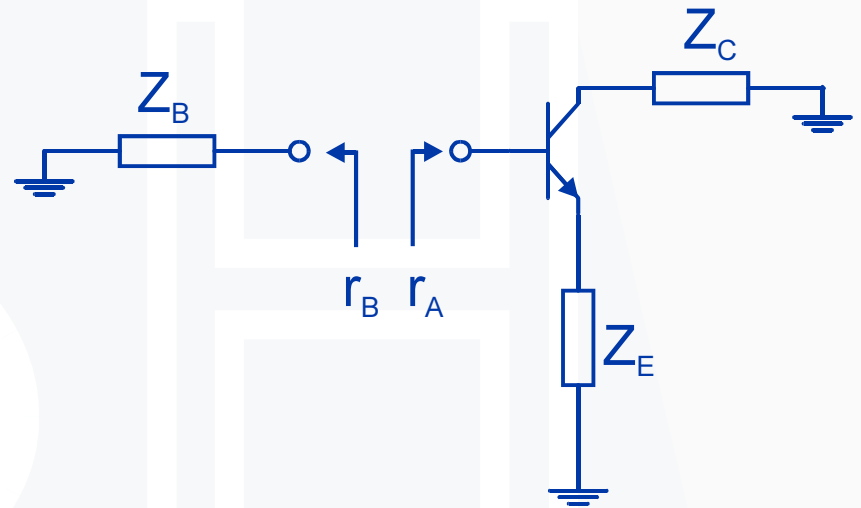
# Problems for low on-chip Q

- no strict separation between amplifier and resonator
- loaded  $Q_L$ 
  - how to define?
  - how to optimize?

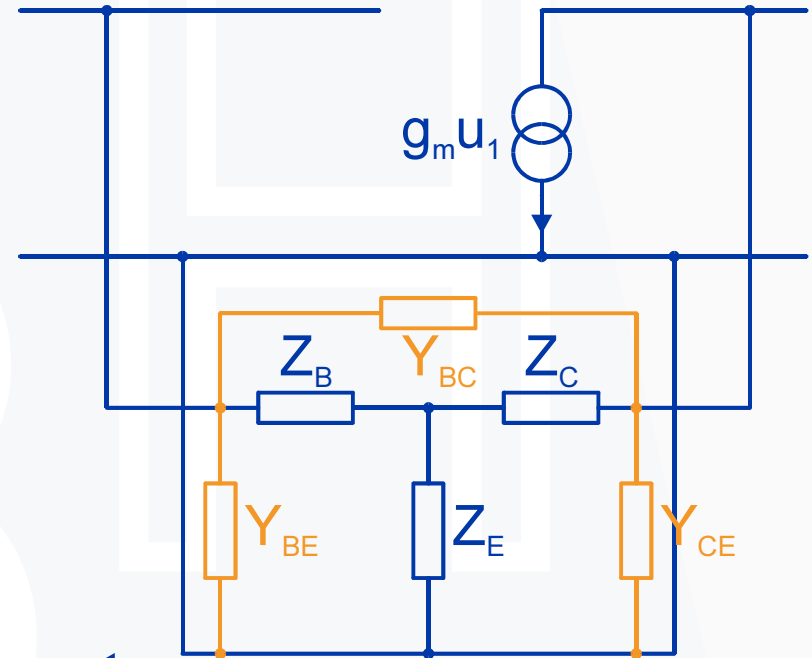
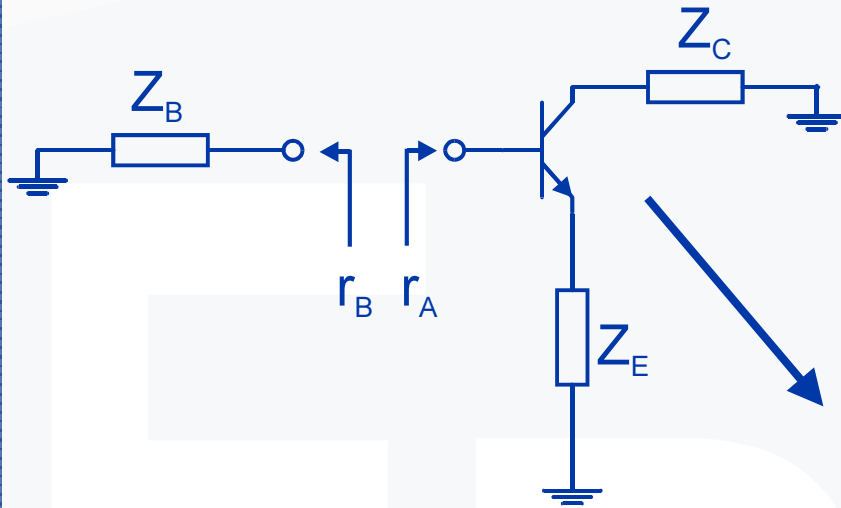
# Loaded $Q_L$ : e.g. reflection-type

- classical microwave oscillator
- 3 impedances
  - $Z_E, Z_C, Z_B$
- 1 active device
- 2 sub-circuits
  - active  $r_A$  / passive  $r_B$
- oscillation condition

$$r_A r_B = 1 + j0$$



# Loop gain calculation

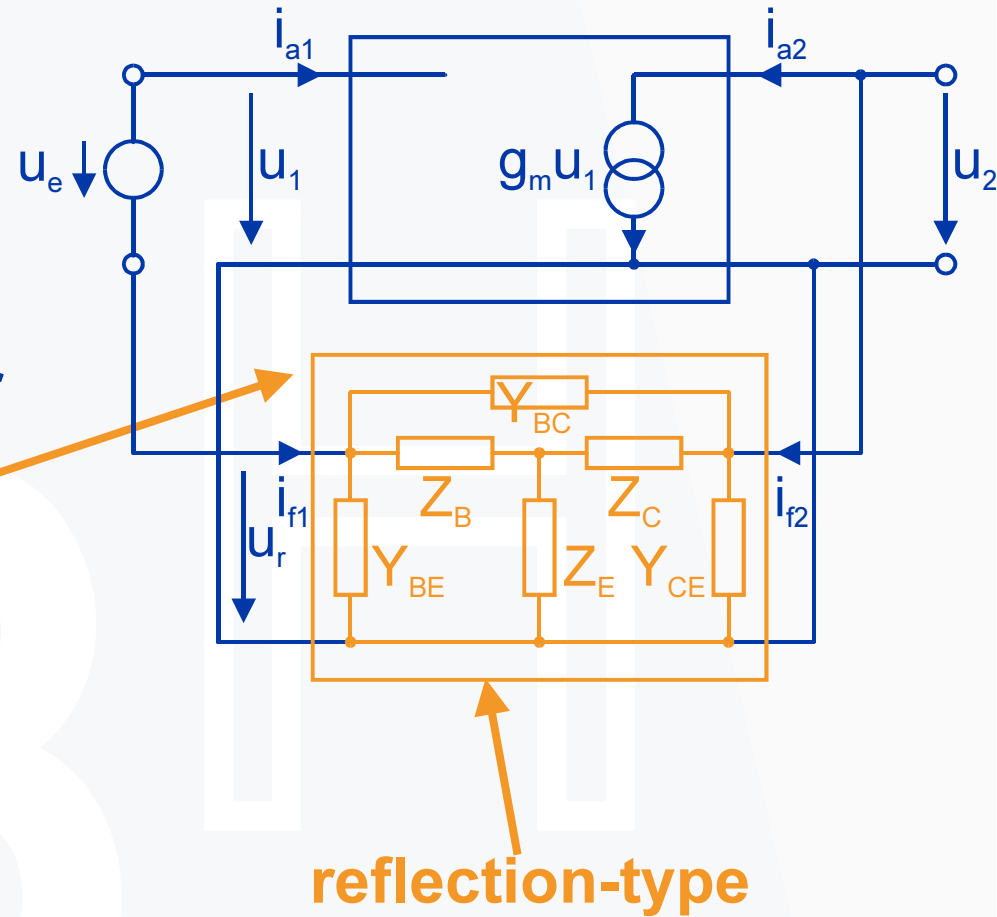


- **rearranging**
  - 2 parallel two-ports
- **equivalent circuit**
- **moving inner elements except for transconductance  $g_m$**

# Loop gain calculation

- circuit topology as desired (see above)
- amplifier reduced to  $(Y_{21}-Y_{12})$  of transistor
- **feedback two-port  $Z_f$**
- effective transconductance  $g'_m$

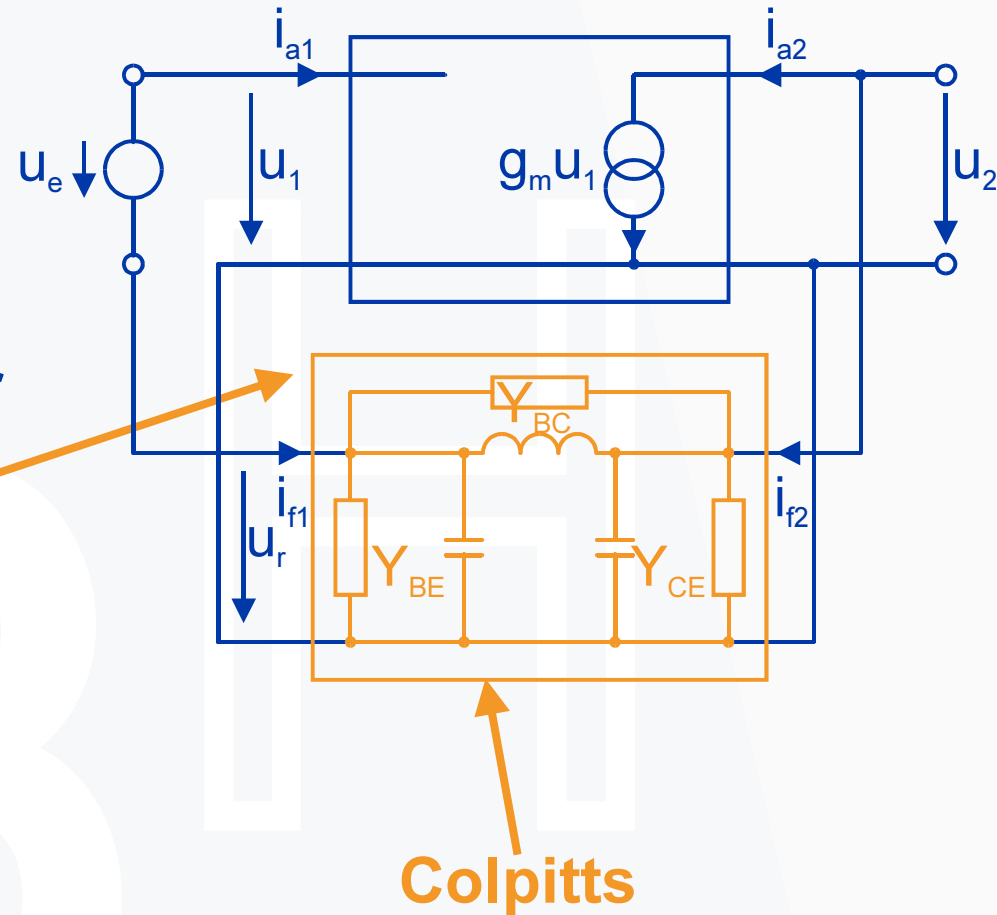
$$g'_m = \frac{i_{a2}}{u_e} = \frac{g_m}{1 + Z_{f12} g_m}$$



# Loop gain calculation

- circuit topology as desired (see above)
- amplifier reduced to  $(Y_{21}-Y_{12})$  of transistor
- **feedback two-port  $Z_f$**
- effective transconductance  $g'_m$

$$g'_m = \frac{i_{a2}}{u_e} = \frac{g_m}{1 + Z_{f12} g_m}$$



## How to maximize loaded $Q_L$

### ■ conditions

- relatively “low” gain  $S_V$
- low unloaded  $Q$  of resonator

$$\begin{aligned}
 Y_x &= Y_{a11} Y_{a22} - Y_{a12}^2 \\
 Y_y &= Y_{a11} + Y_{a22} + 2Y_{a12} \\
 Z_x &= Z_B Z_C + Z_B Z_E + Z_C Z_E
 \end{aligned}$$

### ■ reflection-type oscillator

- 8 knowns (active device):  $Y_{a11}, Y_{a12}, Y_{a21}, Y_{a22}$
- 7 unknowns:  $Z_B, Z_C, Z_E, |S_V|$

### ■ loop gain $S_V$ :

$$|S_V| e^{j\varphi} = g_m Z_{f12} = \frac{(Y_{a21} - Y_{a12})(Z_E - Y_{a12} Z_x)}{1 + Z_x Y_x + Z_E Y_y + Y_{a11} Z_B + Y_{a22} Z_C}$$

# How to maximize loaded $Q_L$

## ▪ problem

- which  $Z_B, Z_C, Z_E$  combination yields highest loaded  $Q_L$ ?
- 7 unknowns: no unique solution

## ▪ assumption

- $Z_B, Z_C, Z_E$  are reactive networks with low loss
- $|r_B| = |r_C| = |r_E| = |r_i|$ , usually  $|r_i| \lesssim 1$

## ▪ now 5 unknowns remaining

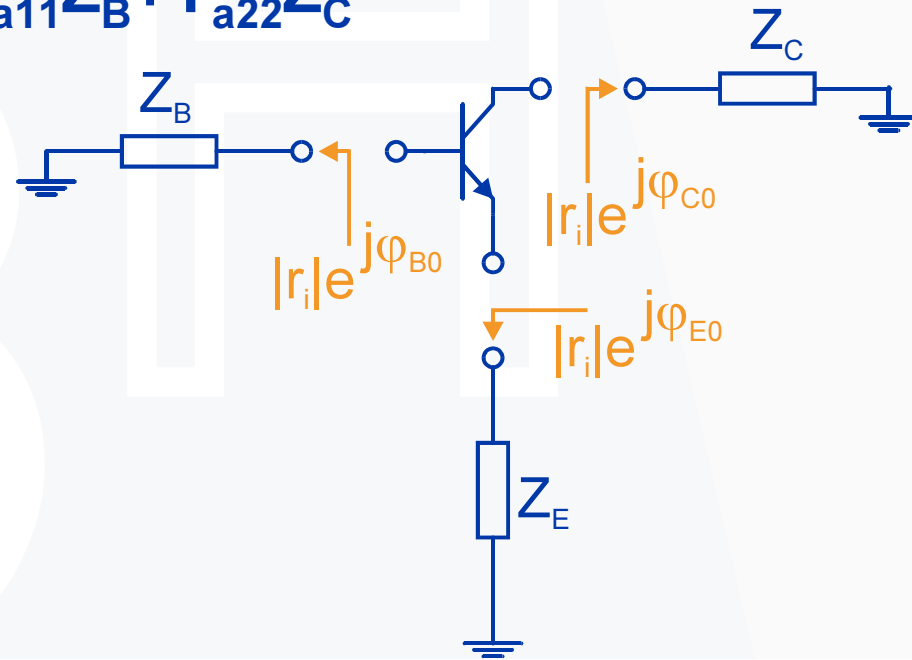
- $\varphi_B, \varphi_C, \varphi_E, |r_i|, |S_v|$

# Loop gain analysis: step I

- fix  $|r_i|$ ,  $|S_v|$  (e.g.:  $|r_i|=0.98$ ,  $S_v = -1.3$ )
- for each  $\varphi_{E0}$  solve (complex) oscillation condition

$$|S_v| e^{j\varphi} = \frac{(Z_E - Y_{a12} Z_x)(Y_{a21} - Y_{a12})}{1 + Z_x Y_x + Z_E Y_y + Y_{a11} Z_B + Y_{a22} Z_C}$$

for  $\varphi_{B0}$  and  $\varphi_{C0}$



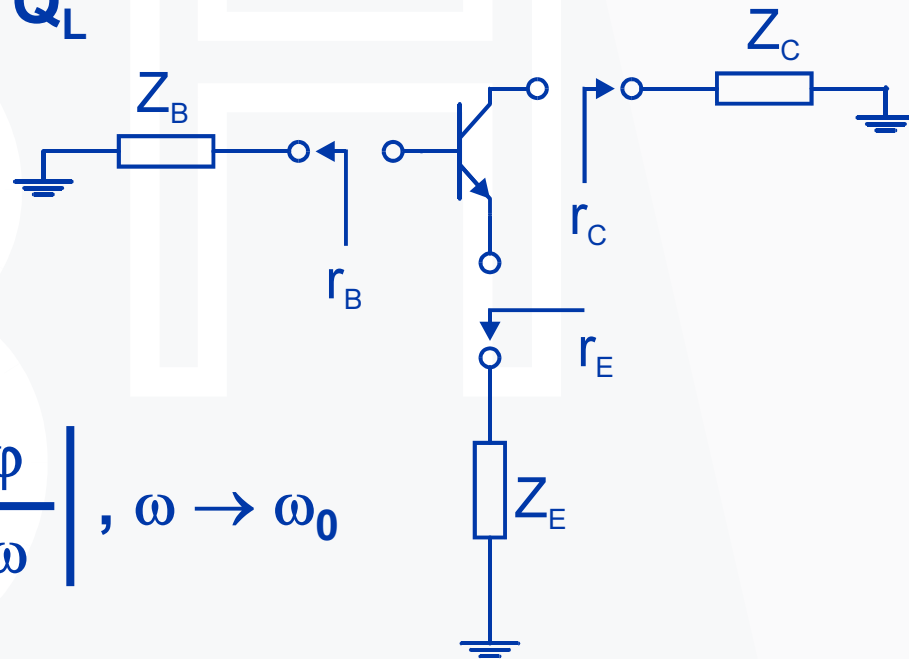
# Loop gain analysis: step II

- add phase slope to  $\varphi_B$ ,  $\varphi_C$  and  $\varphi_E$

$$r_B = |r_i| e^{j(\varphi_{B0} + (\omega - \omega_0) \frac{d\varphi_B}{d\omega})}$$

... to compare the influence of the three branches on loaded  $Q_L$

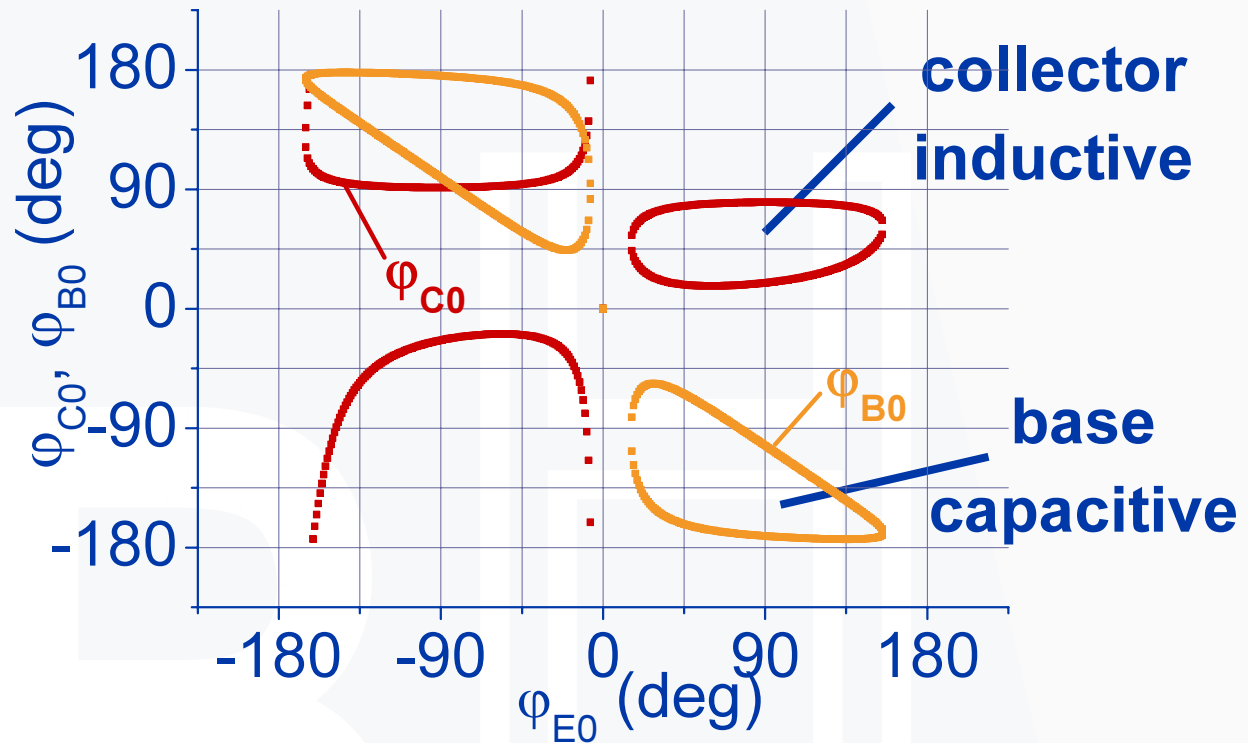
- calculate loaded  $Q_L$  from phase slope of loop gain  
→ find optimum



$$Q_L = \frac{\omega}{2} \left| \frac{d\varphi}{d\omega} \right|, \omega \rightarrow \omega_0$$

# Example: $\varphi_{E0}$ , $\varphi_{B0}$ , $\varphi_{C0}$

emitter  
inductive



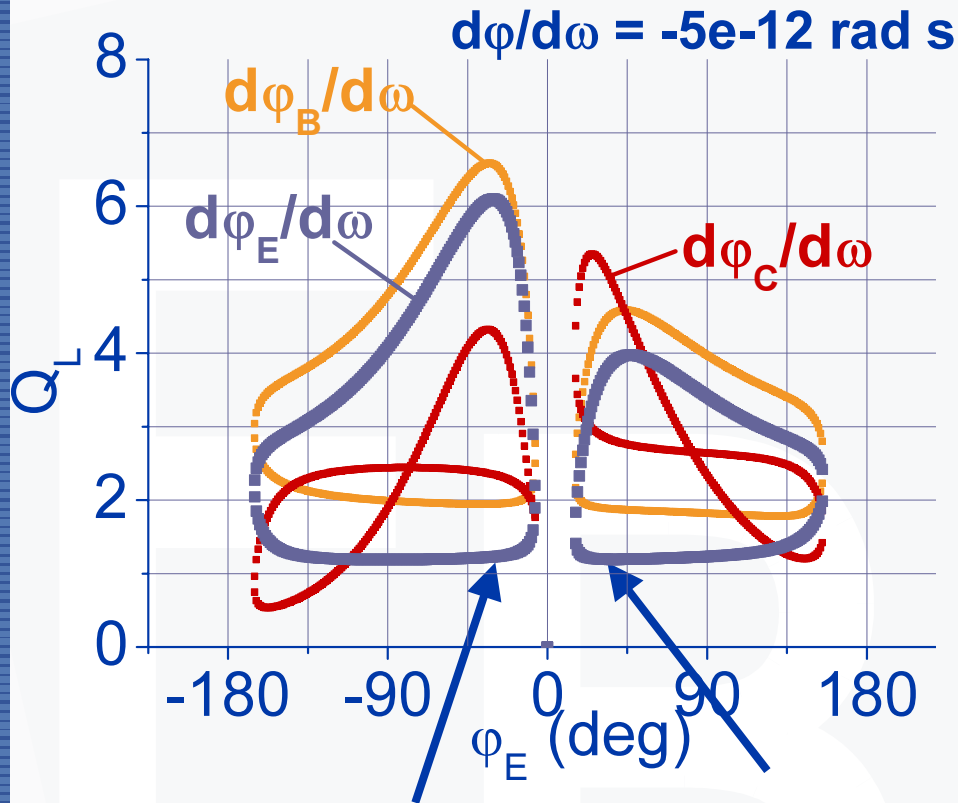
- $f = 38 \text{ GHz}$

- $2 \times 3 \times 30 \text{ } \mu\text{m}^2 \text{ GaAs HBT}$

- $|r_i| = 0.98, S_v = -1.3$

- for each  $\varphi_{E0}$  a pair of  $\varphi_{B0}$  and  $\varphi_{C0}$  exists

# Example: loaded $Q_L$



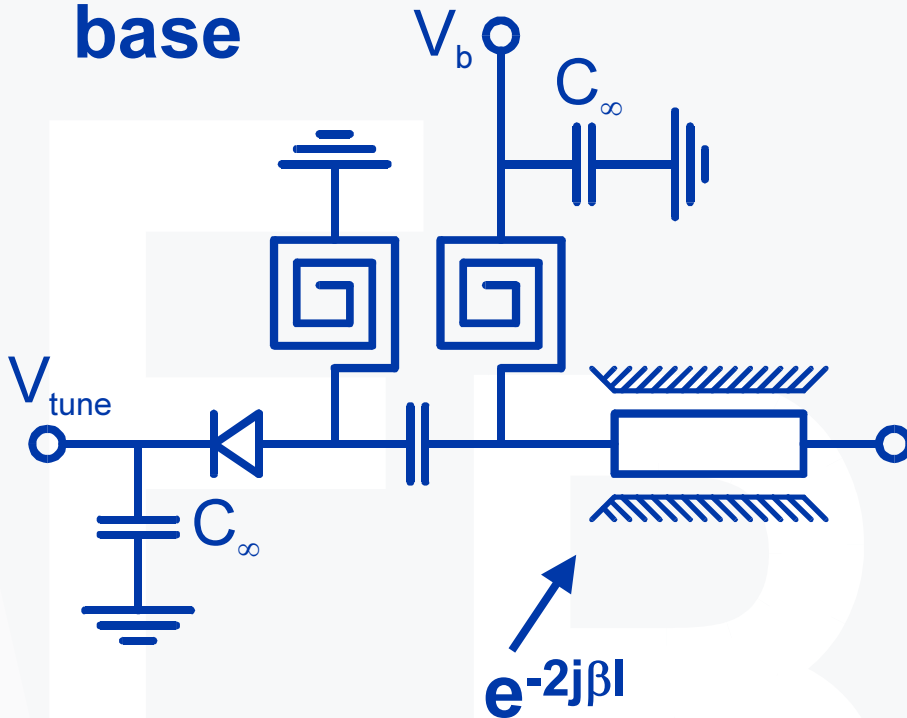
- 3 cases:  
phase slope @ each impedance
- phase slope @ base yields global maximum in  $Q_L$
- best performance @  $\varphi_E \approx -35^\circ, 40^\circ$

e.g.:  $d\varphi_B/d\omega = -5e-12 \text{ rad s}$

$d\varphi_C/d\omega = d\varphi_E/d\omega = 0$

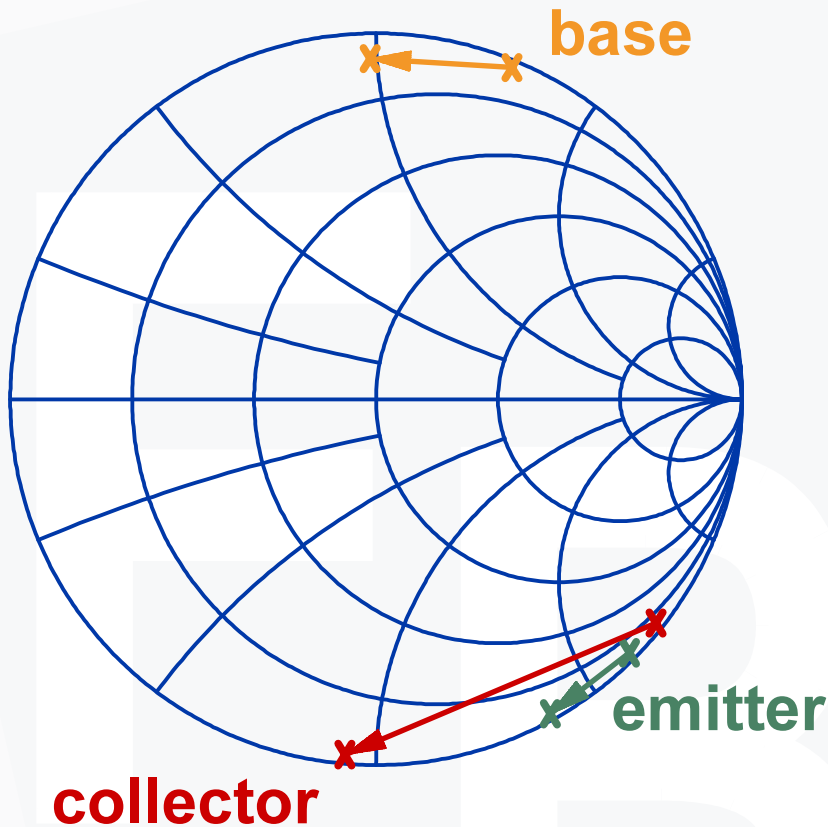
# Circuit design strategy

base



- consider sub-circuit for each impedance  $Z_B$ ,  $Z_C$ ,  $Z_E$  with maximum  $|r_i|$  and phase slope
- adjust optimum phase  $\varphi_B = \varphi_{B0}$ ,  $\varphi_C = \varphi_{C0}$ ,  $\varphi_E = \varphi_{E0}$

# Circuit design strategy

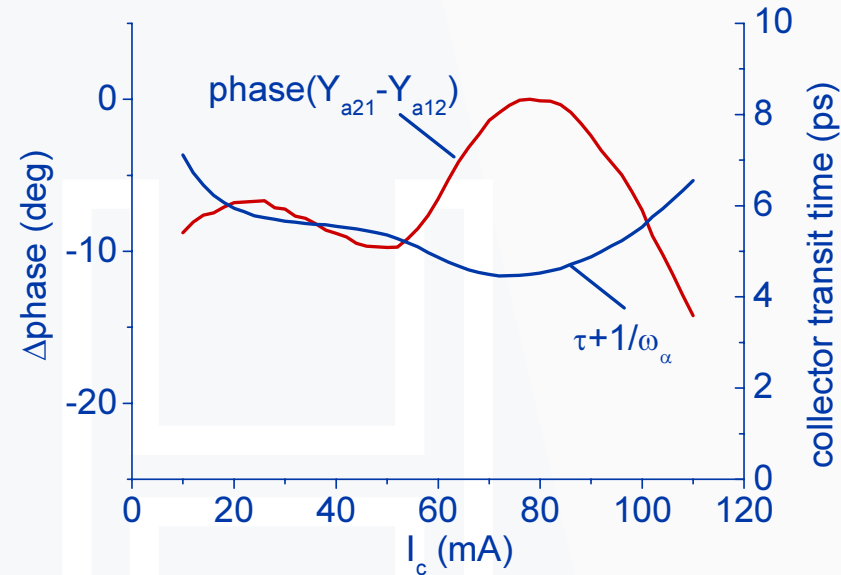


$$S_v = -1.9 \quad |r_i| = 0.98$$

- consider sub-circuit for each impedance  $Z_B, Z_C, Z_E$  with maximum  $|r_i|$  and phase slope
- adjust optimum phase  $\varphi_B = \varphi_{B0}, \varphi_C = \varphi_{C0}, \varphi_E = \varphi_{E0}$
- simulate loaded  $Q_L$
- phase fine-tuning to account for  $|r_B| \neq |r_C| \neq |r_E| \neq |r_i|$

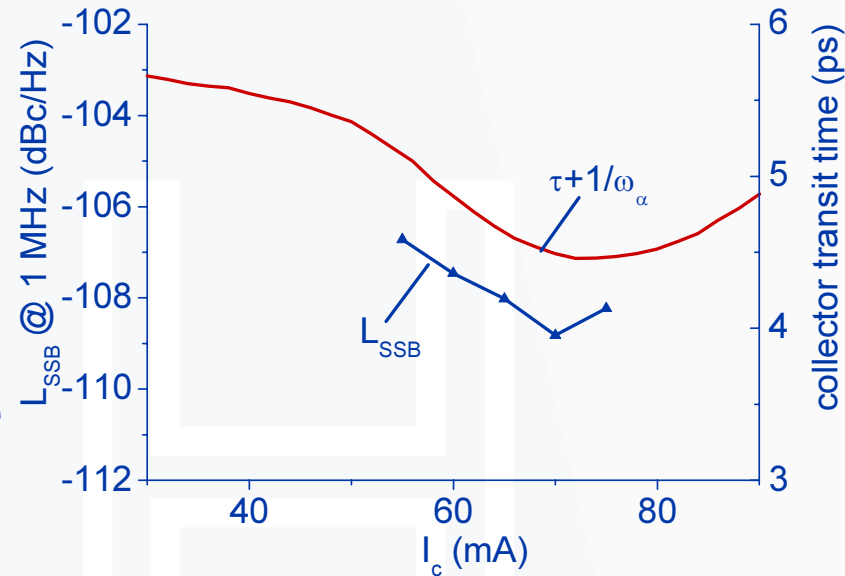
# Bias dependence (GaAs HBT)

- **1/f noise**  $\propto I_C$ 
  - lowest  $I_C$  yields best phase-noise?
  
- **Kirk effect @ high current**
  - maximum  $f_{\max}$
  - minimum collector transit time
  - flat phase of  $g_m = Y_{a21} - Y_{a12}$

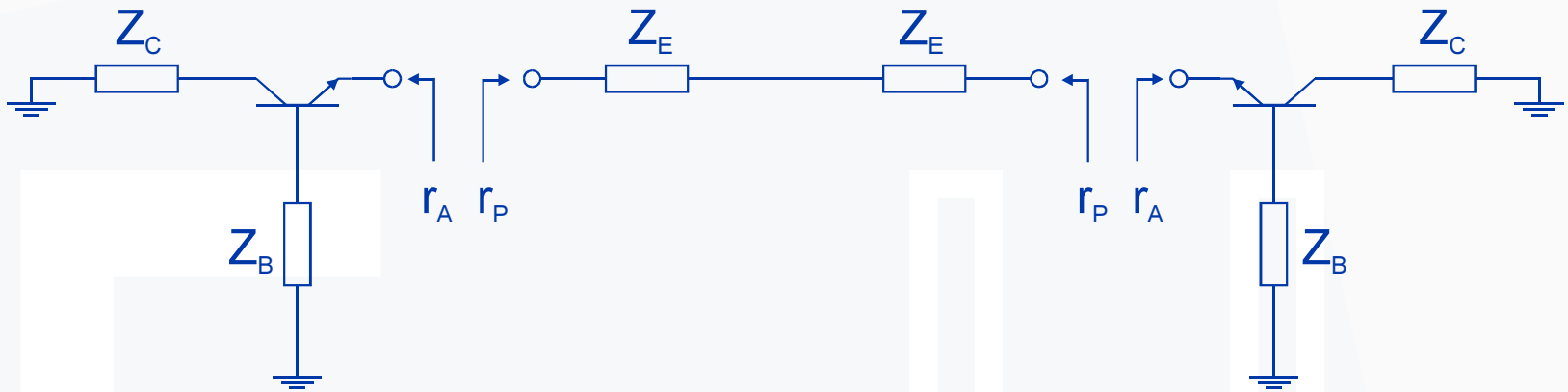


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- **1/f noise  $\propto I_c$** 
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- **Kirk effect @ high current**
  - maximum  $f_{max}$
  - minimum collector transit time
  - flat phase of  $g_m = Y_{a21} - Y_{a12}$
- **minimum phase-noise @ Kirk-current**  
-> high-current regime superior

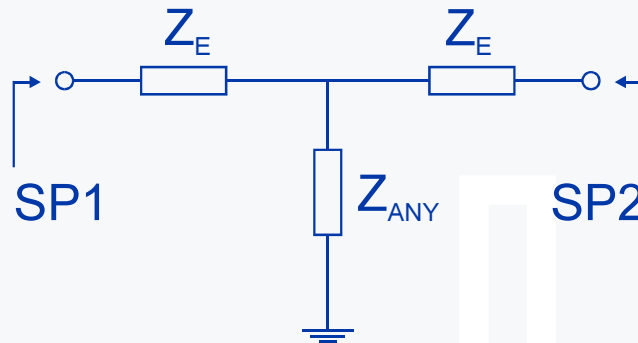


# Push-push concept



- reflection-type oscillator
- 3 impedances to ground
- oscillation condition:
  - $|r_p r_a| > 1$
  - $\text{phase}(r_p r_a) = 0$
- connection in former ground node
- two modes possible:
  - ODD mode
  - EVEN mode

# Push-push oscillators : ODD mode



- **ODD mode**

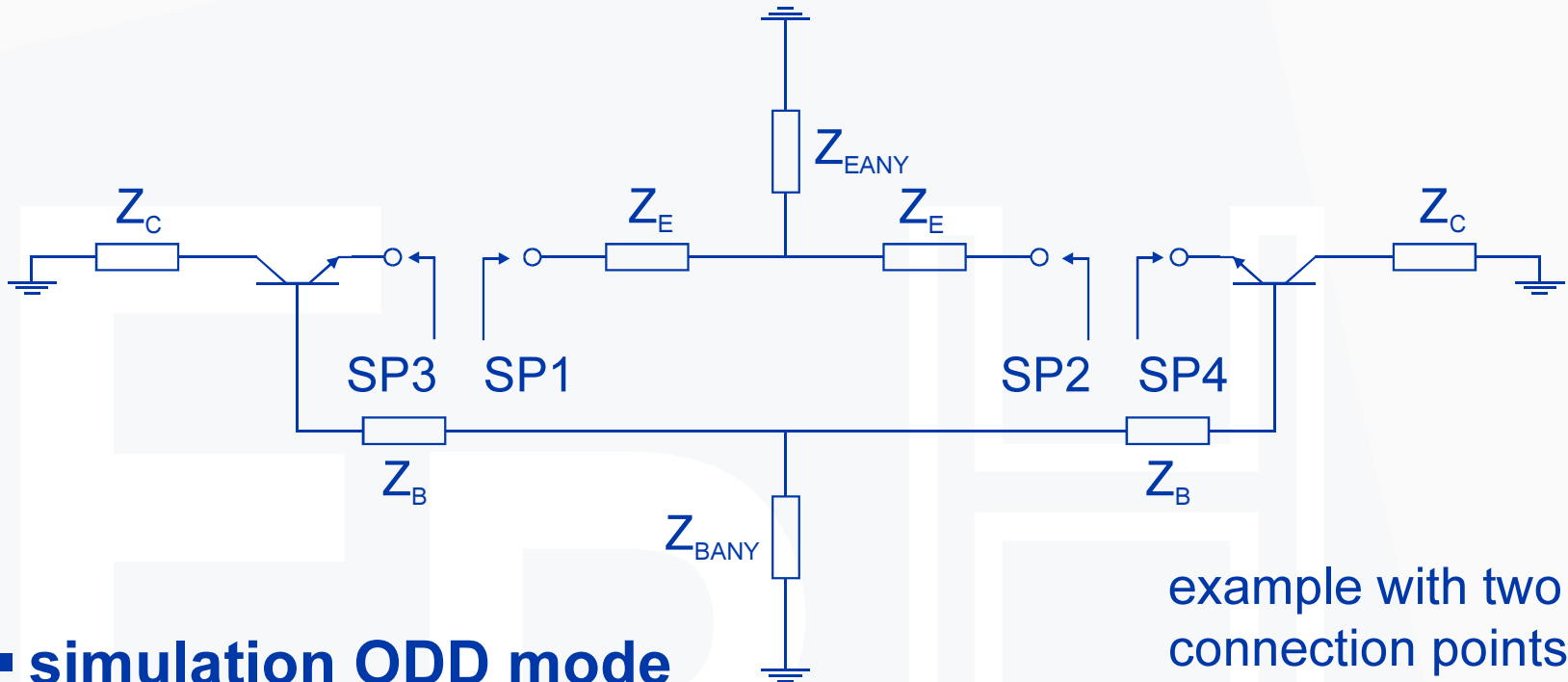
- virtual ground in connecting point
- fundamental cancels, 2nd harmonic interferes constructively

- **$Z_{ANY}$  for DC-supply and / or output**

- **e.g.: output**

- open @ fundamental (mode separation)
- match @ 2nd harmonic

# Push-push oscillators : simulation



- **simulation ODD mode**

- $r_P r_A = (S_{11} - S_{12}) (S_{33} - S_{34})$

- **simulation EVEN mode**

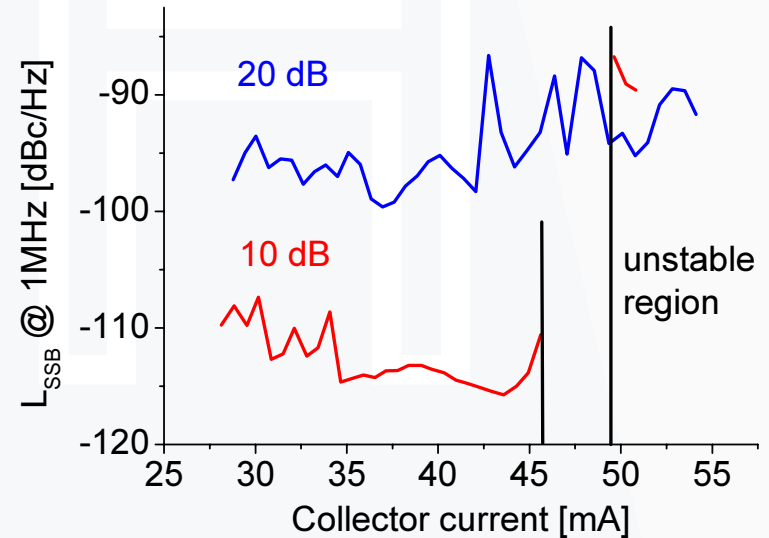
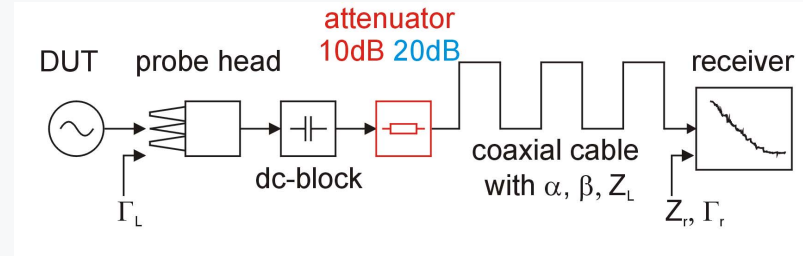
- $r_P r_A = (S_{11} + S_{12}) (S_{33} + S_{34})$

# Push-push oscillators: advantages

- **higher device gain @  $f_{osc}/2$** 
  - higher loaded  $Q_L$  possible
- **output-load not effective @ fundamental**
  - less gain reduction
  - less  $Q_L$  reduction
  - less load pulling
- **noise reduction due to transistor coupling (“3 dB”)**
- **experience: phase noise reduction compared to doubler concept**

# Measurement: load-pull effect

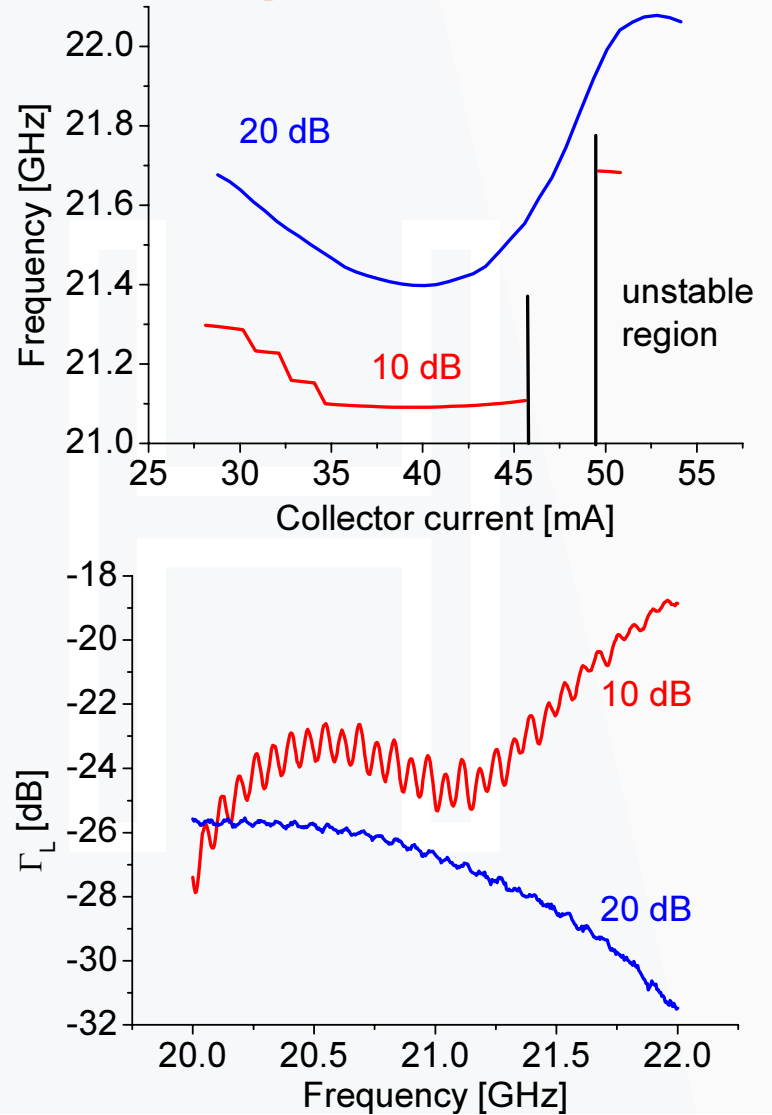
- insufficient isolation affects phase noise measurement
- measurement system becomes part of the oscillator
- low on-chip  $Q_L$ 
  - phase noise sensitive to measurement environment



# Measurement: typical tuning curve

- **20 dB attenuator:**
  - smooth tuning curve
- **10 dB attenuator:**
  - distinct frequency plateaus (70MHz distance)

reflection coefficient  
 $\Gamma_L$  of setup



# Be aware of load-pull effects!

## ▪ for measurement:

- always monitor tuning curve!

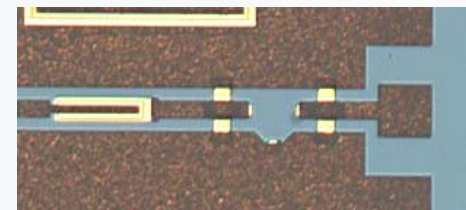
## ▪ for measurement setup:

- keep receiver mismatch small (isolator)
- use attenuators
- use keep interconnection short (or very long)

## ▪ for circuit design

- use buffer or on-chip attenuators
- if not: choose weak output coupling

on chip attenuator



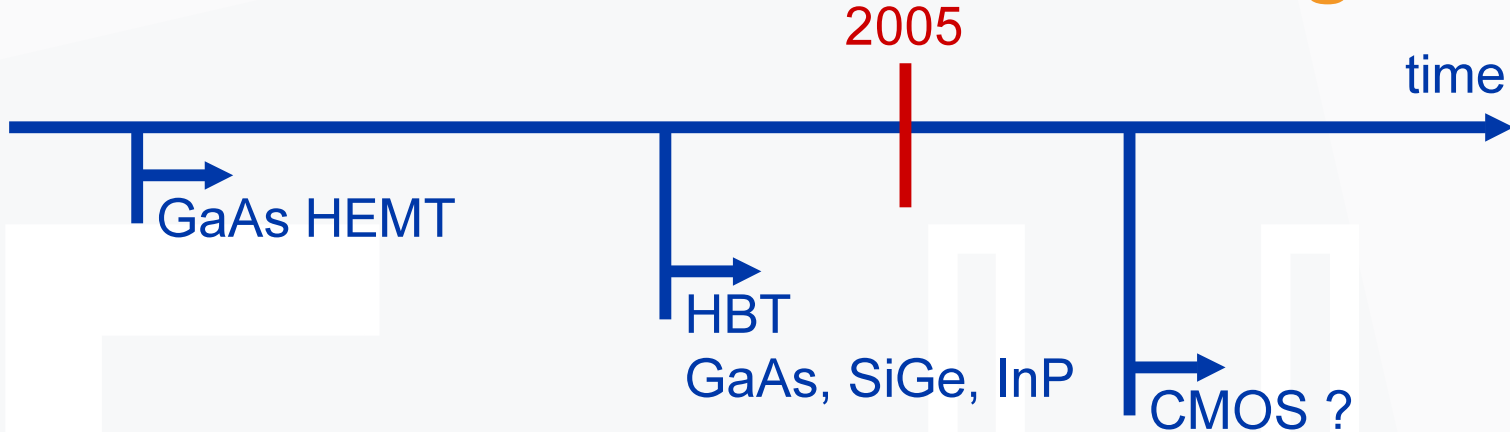
# Remarks on phase-noise simulation

- **oscillator simulation for  $\mu$ - and mm-wave**
  - Time-Domain difficult
  - Harmonic Balance (ADS, Serenade,  $\mu$ wave Office, ...)
- **phase noise simulation: our experience (GaAs HBT)**
  - results not reliable
    - ▶ difficulties with user-defined models
    - ▶ agreement with measurements mostly unsatisfactory
  - reasons: analysis method and/or transistor model ?
- **situation may be different for SiGe HBT**

# MMIC VCOs: design rules summary

- **optimize loaded  $Q_L$  (consider parasitics)**
- **device with high gain**
  - circuit becomes insensitive to device parasitics
  - allows for loose coupling of resonator and thus high loaded  $Q_L$
- **differential / push-push configuration**
- **optimize bias point**  
(GaAs HBT: high current regime advantageous)

# mm-wave MMIC VCOs: technologies



	GaAs HEMT	GaAs HBT	SiGe InP HBT	CMOS
mm-wave "experience"	+++	++	++	+
oscillation frequency	+++	++	+++	+
1/f noise phase-noise	+	+++	+++	++

commercially available

upcoming

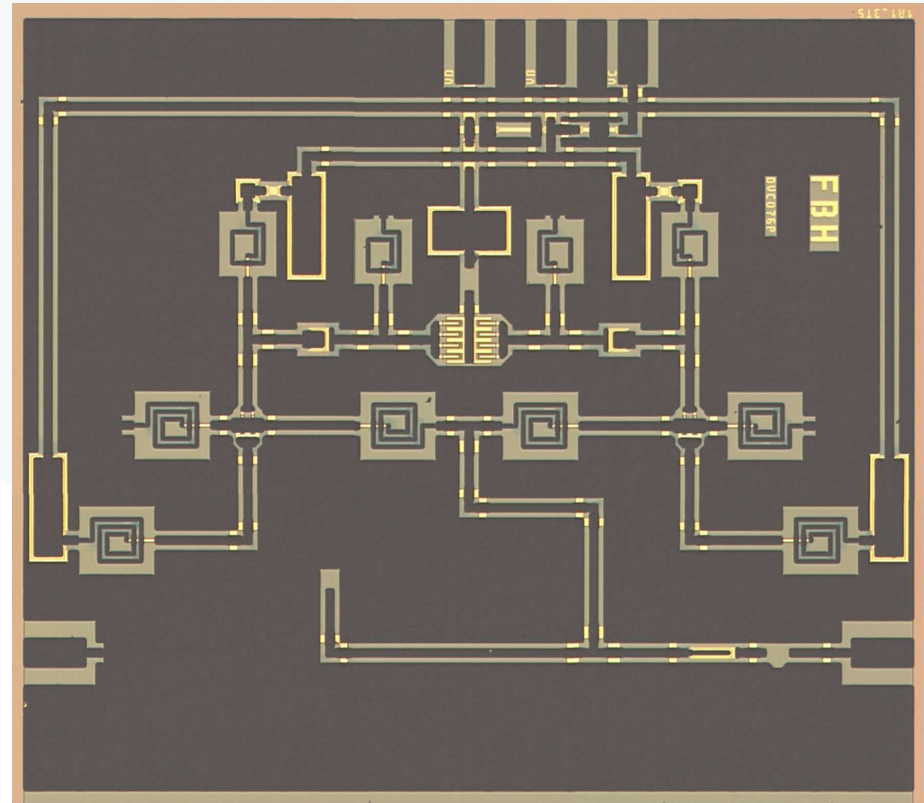
# Recent advances mm-wave VCOs

## ▪ HBT MMIC (GaAs, SiGe, InP)

- dominant in publications of last years
- every year new record values regarding
  - ▶ frequency ( $f_{\text{osc}} / f_{\text{max}}$ )
  - ▶ phase-noise
  - ▶ or both
- GaAs HBT now commercially available (up to 38 GHz)
- SiGe upcoming

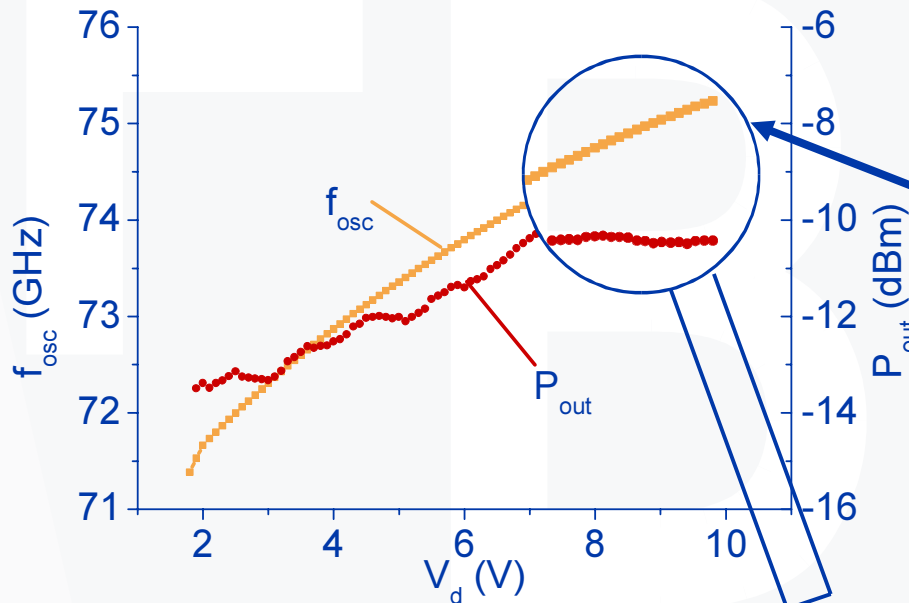
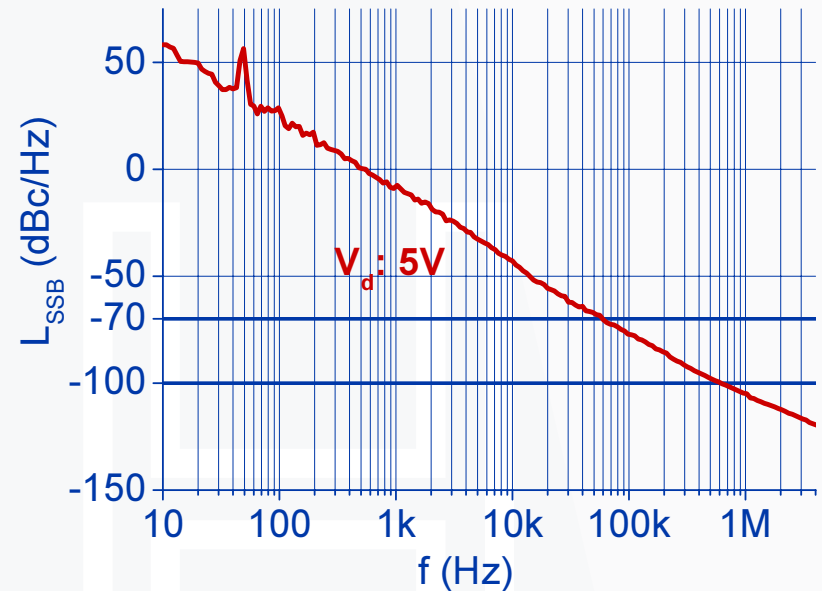
## Example: W-band VCO with GaAs HBT

- Lenk et al., 2004 (FBH)
- optimized phase condition for max. loaded  $Q_L$  @ 38 GHz
- two virtual grounds (base + emitter)
- $2.2 \times 1.9 \text{ mm}^2$
- push-push



# Example: W-band VCO with GaAs HBT

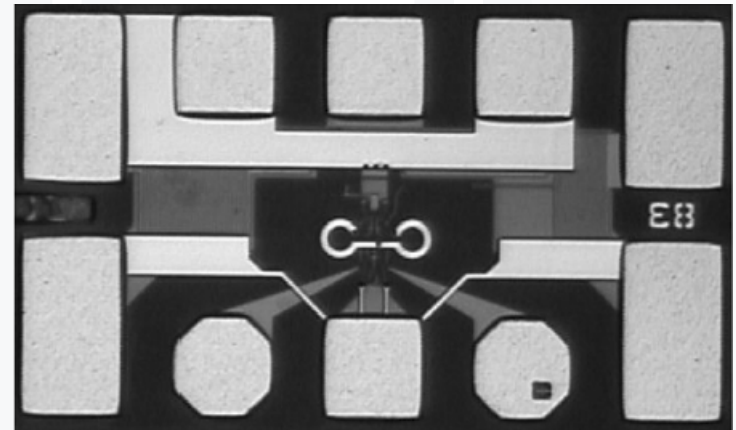
- output power:  $> -5$  dBm
- $f_{osc}$ : 73.6 GHz, 5 % tuning
- low phase noise  
(-105 dBc/Hz @ 1 MHz)



no steps in frequency  
 $\Delta V_d = 0.1 V$

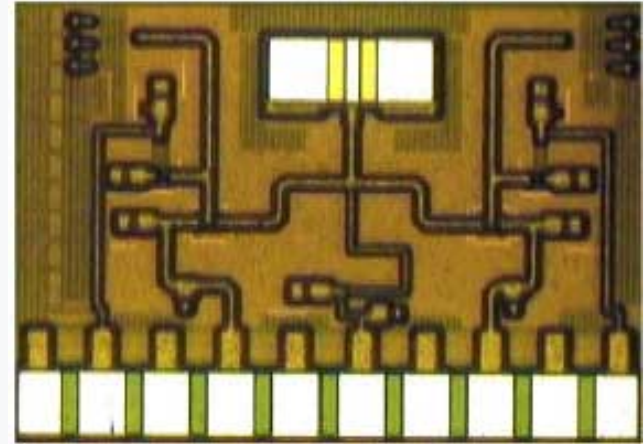
## Example: W-band VCO with InP HBT

- Zhihao Lao, et al., 2004 (HRL)
- described as Colpitts concept
  - nC capacitor realized with  $C_{BE}$
- output power: -1 dBm
- $f_{osc}$ : 80 GHz, 5 % tuning
- low phase noise  
(-118 dBc/Hz @ 1 MHz)



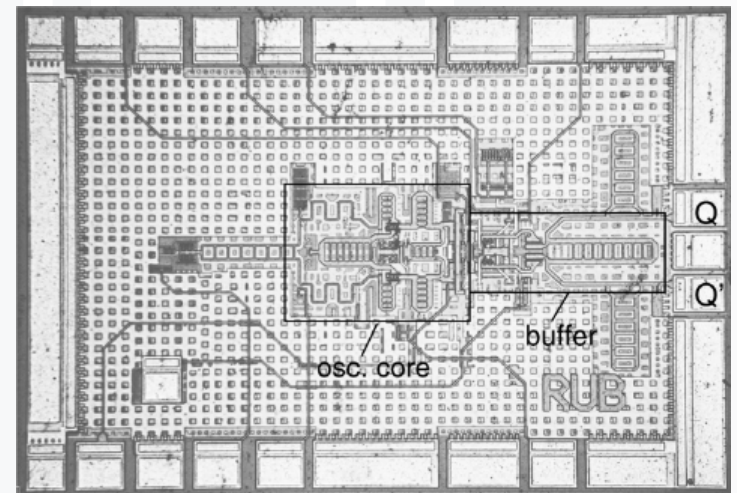
## Example: W-band VCO with SiGe HBT

- **Steinhauer, et al., 2004**  
(Bosch, FBH, IBM process)
- **reflection-type oscillator**
- **output power:  $\approx 0$  dBm**
- **$f_{\text{osc}}$ :**
  - 107 GHz, 7 % tuning (fundamental)
  - 110 GHz, 14 % tuning (push / push)
- **low phase noise**  
(-90 dBc/Hz @ 1 MHz)



## Example: W-band VCO with SiGe HBT

- Hao Li, H.-M. Rein, T. Suttrop, J. Böck\*  
(Bochum University, \*Infineon)
- differential coupled reflection-type oscillator
- output power:  $\approx 18.5$  dBm
- $f_{\text{osc}}$ : 77 GHz, 8.7 % tuning
- low phase noise  
(-97 dBc/Hz @ 1 MHz)

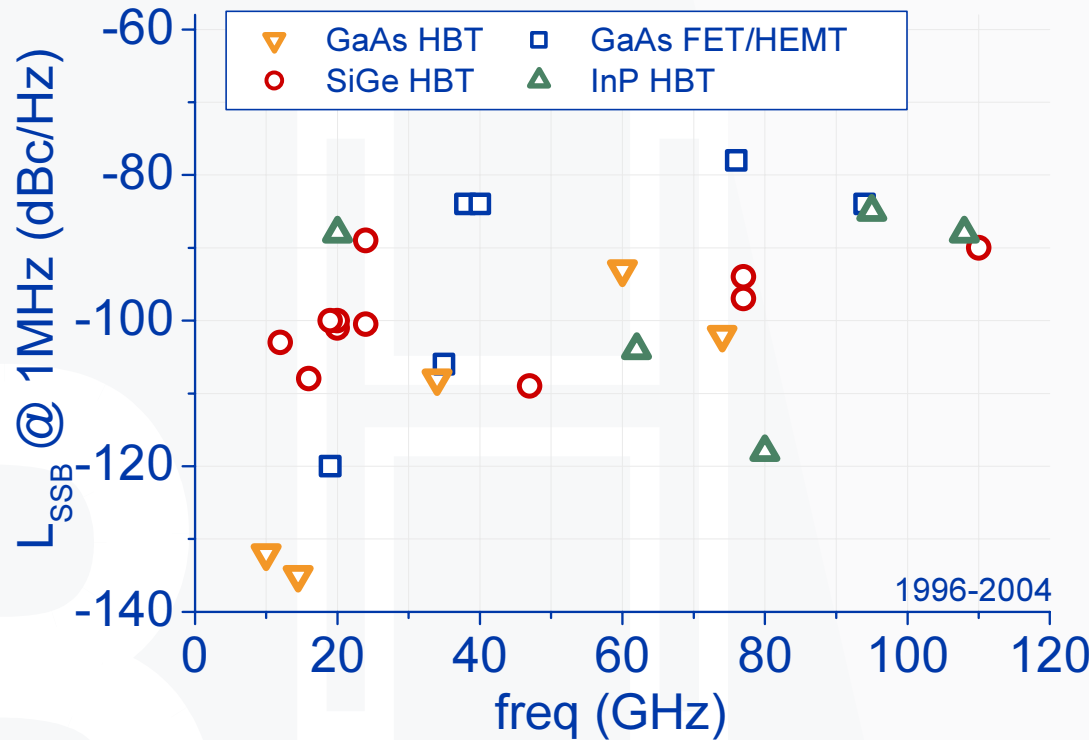


## Example: CMOS VCO

- F. Ellinger, et al., 2004  
(ETH Zürich, IBM process)
- cross-coupled differential LC oscillator
- output power:  $-6.8$  dBm
- $f_{\text{osc}}$ : 56.5 GHz, 14 % tuning
- phase noise  
( $-90$  dBc/Hz @ 1 MHz)

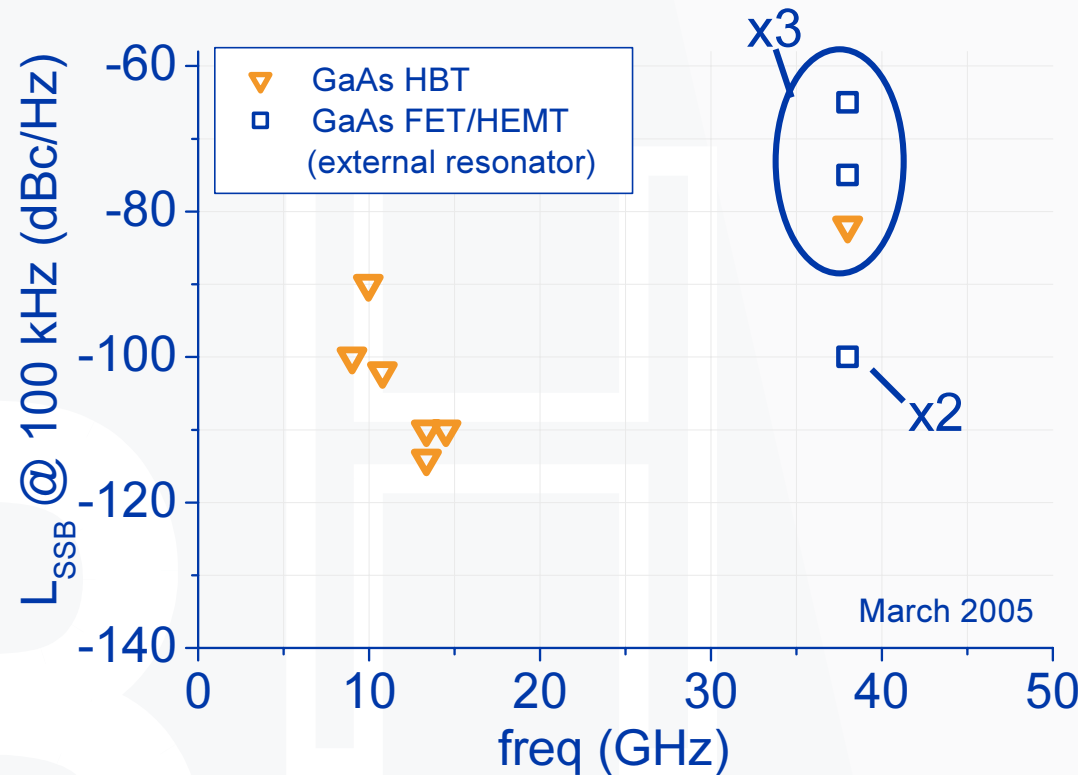
# Benchmarking: research results

- published data since 1996
- SSB phase noise @ 1 MHz offset
- only fully monolithic circuits
- HBT dominant



# Benchmarking: commercial availability

- presently only GaAs
- SSB phase noise @ 100 kHz offset
- HEMT
  - external resonator
- HBT
  - fully monolithic
  - mostly push-push
  - above 20 GHz: multiplier concept



# mm-wave MMIC VCOs: the future I

## ■ technologies

- HBT devices will make the race, critical issues:
  - ▶ SiGe: W-band power?
  - ▶ GaAs: frequency limit?
  - ▶ InP: cost & availability
- CMOS performance not yet clear
- advance depends on market demands
  - ▶ communications (40 GHz): -110 dBc/Hz @ 100 kHz
  - ▶ W-band radar: -70...-90 dBc/Hz @ 100 kHz

# mm-wave MMIC VCOs: the future II

## ▪ hybrid / monolithic

- fully monolithic MMIC will gain ground
- discrete (MIC) VCO only for small quantities
- cavity VCO for extremely low phase-noise

## ▪ situation may change completely

- if monolithic high Q-resonators are possible
  - ▶ Micromachining / MEMS?

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## ▪ Benchmark: GaAs HEMT

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## ▪ Benchmark: Commercial VCOs

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