Low Phase-Noise GaAs-HBT Monolithic W-Band Oscillator

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***Abstract* — A W-band MMIC VCO using GaInP/GaAs HBTs is presented. It achieves a wide tuning range of 5 % and a SSB phase noise of -102 dBc/Hz at 1 MHz offset frequency. To our knowledge, this is the first fully monolithic VCO in this frequency range with a 1 MHz-offset phase-noise value better than -100 dBc/Hz.**

I. INTRODUCTION

Low phase-noise oscillators are key components in each mm-wave communications or sensor system. For higher volume applications such as automotive radar, a fully monolithic solution is necessary in order to meet cost restrictions. For GaAs HEMT devices, due to the high 1/f-noise, only approaches with external resonator or injection locking [1] achieve acceptable phase-noise performance.

Hence, for fully monolithic VCOs, HBT devices are preferable. They combine high transit frequency with low 1/f-noise. Starting with InP technology [2], in the meantime also GaAs [3] and even SiGe [4] based VCO MMICs have been presented, which yield comparable performance regarding frequency, output-power, and phase-noise. This suggests that for HBT oscillator circuits in this frequency range, the loaded Q_L of the circuit is dominant for phase-noise performance.

In this paper, we present a push-push oscillator using GaInP/GaAs HBTs in a coplanar MMIC environment. It consists of two identical fundamental oscillators combined in a virtual ground node, where the second harmonic is extracted. A second combining point is introduced to prevent even-mode oscillation at lower frequencies. The fundamental oscillator is optimized for high loaded Q_L using the technique described in [5].

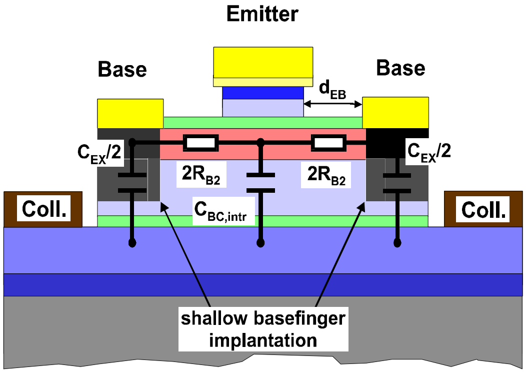

Fig. 1. Scematic image of an InGaP/GaAs-HBT after collector metallization.

II. TECHNOLOGY

For low phase-noise VCOs in W-band, the active devices must combine high gain at the operating frequency with low 1/f noise. For this reason, we use InGaP/GaAs HBTs as active element, which also provides low-loss substrate properties. The epitaxial layers are grown by Metalorganic Vapor-Phase Epitaxy (MOVPE). The HBT-structure consists of a 55 nm n^+-InGaAs emitter-contact-layer, a 100 nm thick n-GaAs layer, a 30 nm n-InGaP emitter and a 100 nm uniformly doped p-GaAs base layer, an 1 µm n-GaAs collector, a 20 nm GaInP etch stop layer and a 700 nm thick n^+-GaAs subcollector. Si is used for n-doping, intrinsic carbon doping is applied for the p^+-base layer ($p = 4*10^{19}$ cm^{-3}). The β_{max}/R_{SBI}-ratio of jumbo-HBTs is determined to be 0.5 $(\Omega/sq)^{-1}$ which indicates a very good epitaxial material quality.

The HBT MMICs are fabricated on our industry-compatible 4" process line with stepper lithography. The process comprises a total of 14 lithography levels.

In order to increase the maximum frequency of oscillation f_{max} (and thus the available gain of the HBT at the operating frequency), both the base resistance R_B and the total base-collector capacitance $C_{BC,intr} + C_{EX}$ (see Fig. 1) have to be reduced: Shrinking the distance between the base finger and the emitter d_{EB} a significant reduction of R_B ($R_{CB} + R_{B2}$) can be achieved (see Fig. 1). Scaling down d_{EB} from 1.3 µm to 0.5 µm R_B decreased by 47 %, resulting in an f_{max} increase from 95 to 150 GHz.

To keep the parasitic base-collector capacitance C_{EX} low we implemented a shallow base-finger implantation. So, the parasitic layer of the base region and roughly 80 % of the upper part of collector in the outer basefinger area are isolated. This leads to a reduction of $C_{BC} = C_{BC,intr} + C_{EX}$ by 44 %. In summary, together with a down-scaled d_{EB} as described above, f_{max} could be increased from 95 to 170 GHz.

Regarding 1/f-noise it has to be mentioned that neither the shallow base-finger implantation nor the d_{EB} reduction has an impact on low-frequency noise. Obviously, a base-finger emitter spacing of 0.5 µm is not critical and lateral diffusion of electrons from the emitter to the base contact does not occur. Otherwise, a higher base current and thus an increased 1/f noise would have been detected.

In order to prevent emitter-base surface leakage currents and thus additional 1/f noise, ledge technology is applied. As passive elements, MIM capacitors (dielectric material: SiN_x), thin film resistors (NiCr), spiral induc-

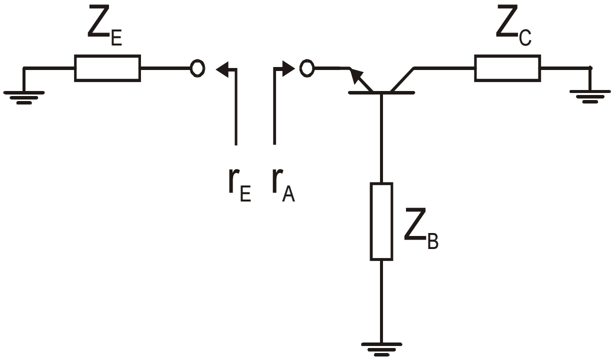

Fig. 2. Circuit topology of a reflection-type oscillator.

tors, coplanar waveguides, and air bridges (electroplated Au) are used. For further details of our MMIC process see [6].

III. CIRCUIT DESIGN

The fundamental oscillator is designed as a reflection-type circuit as shown in Fig. 2. Three impedances Z_E, Z_C and Z_B are connected to the transistor ports. These impedances are representing both the bias networks and the varactor diode. With the design strategy proposed in [5] a optimum phase condition is found to achieve highest loaded Q_L. For this circuit the phases are: $\varphi_E = -58°$, $\varphi_C = -100°$, and $\varphi_B = 90°$ (simulated values).

To maximize the loaded Q_L of the circuit all of the three impedances should provide a maximum of phase slope and a reflection-coefficient magnitude near unity at resonance frequency to the transistor ports. At emitter and collector, similar structures are used to adjust the desired phases. RF ground is realized with the block capacitor at the collector and with the virtual ground at the emitter. From the ground, a spiral inductor with two turns transforms the phase by λ/4. With coplanar waveguides (CPW), the remaining phases are adjusted to meet the optimum phase condition stated above.

At the emitter port, a second spiral inductor (also used as λ/4 transformer) provides the dc connection. Because the phase transformations start from ground and lead to negative phase values, the transformed phase in total is larger than 180°. Therefore, the oscillation phase condition is fulfilled several times and special attention is needed to avoid spurious oscillations. At the bases, a two-stage block capacitor with a resistor in series is used to prevent oscillation in the lower GHz range by reducing the available loop gain. Furthermore, the varactor diode is included in the base branch, because this provides the largest tuning bandwidth. Again spiral inductors und CPWs are used to adjust the desired phase. The varactor diode is not DC decoupled from the base of the transistor to achieve a better linearity in the tuning characteristic.

Because of the large phase transformations at all ports of the active device we pay special attention to prevent even mode operation of the circuit. Simulating the coupled circuit rather than the half-structure, even and odd mode can be separated as shown in [3] with:

$$\begin{aligned} r_{odd} &= S_{11} - S_{12} \\ r_{even} &= S_{11} + S_{12} \end{aligned} \qquad (1)$$

The product of the reflection coefficients from active and passive part of the circuit is considered, because it indicates possible oscillations for both modes. For loaded Q_L maximization, only the half structure is optimized.

The output is connected to the virtual ground in the emitter connection of the fundamental oscillators. A similar transformation as shown in [3] is used to provide an open circuit at the fundamental frequency and a 50 Ω load at the second harmonic. A second connection of the two fundamental oscillators is realized at the varactor diodes. This is to prevent a possible even mode oscillation in a frequency range nearby the desired frequency. A 10 dB attenuator at the output decouples the oscillator from the measurement environment during on-wafer

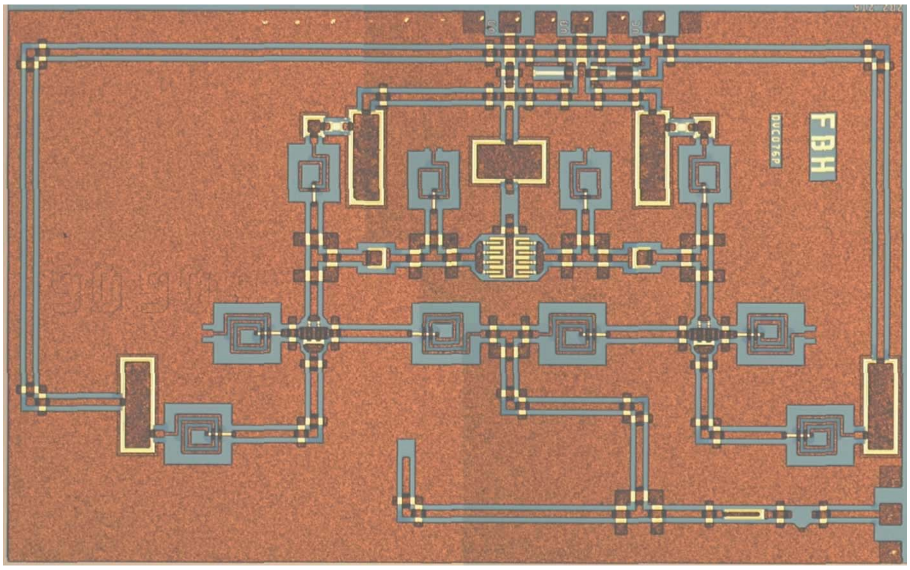

Fig. 3. Chip photo of the MMIC oscillator (size: 1.5 x 2.4 mm^2).

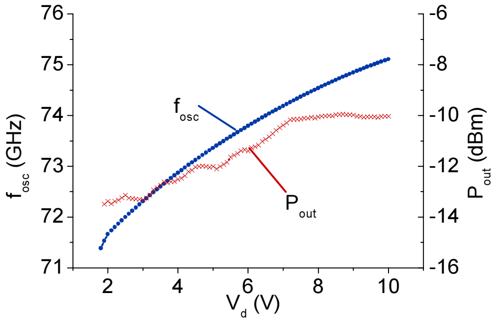

Fig. 4. Tuning characteristics of the W-band VCO: frequency of oscillation and output power against tuning voltage.

probing, which suppresses load-pull effects.

III. MEASUREMENTS

The measurements are performed using the E5504 phase-noise measurement system from Agilent. A one-way circuit is used to optimize the load seen from the oscillator. After mixing the signal with a 67 GHz Gunn oscillator, the phase noise is characterized applying the delay-line method. Power is measured using a HP W8486A power sensor. In Fig. 4, the tuning characteristics of the oscillator is shown. Small tuning steps of ΔVd = 100 mV are used to detect possible curve discontinuities (steps) due to load-pull effects. The circuit shows stable oscillation between $71.4 < f_{osc} < 75.1$ GHz which corresponds to a relative tuning bandwidth of $\Delta f_{osc} = 5$ %. The measured power P_{out} is in the range -15…-10 dBm. Using the VCO in a system, the on-chip attenuator can be omitted, which results in 10 dB more output power.

In Fig. 5, the measured phase-noise data is plotted. At all varactor bias points, the phase-noise is lower than -100 dBc/Hz at 1 MHz offset frequency and lower than -70 dBc/Hz at 100 kHz, respectively. Note that this -30dB/dec slope differs from the SiGe HBT case where usually –20dB/dec are observed at comparable offset frequencies.

At 100 kHz offset frequency, the curve shows a bump that resembles effects caused by generation-recombination noise.

To investigate this in more detail, additional phase-noise measurements were performed at the fundamental frequency, where the measurement set-up does not require the Gunn oscillator for down-conversion. Instead, the HP 8350 with 40 GHz plug-in is used to mix the signal down to the range of 12 GHz. A 25 dB amplifier is needed to provide sufficient signal power.

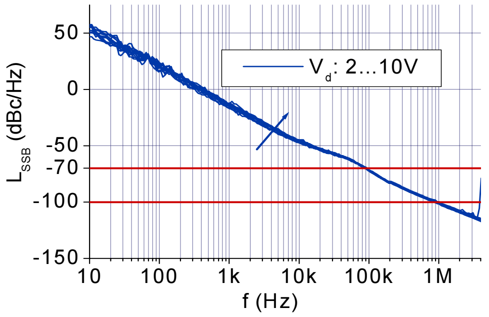

Fig. 5. Phase-noise measurements with tuning voltage V_d = 2...10 V as parameter (1 V steps): SSB phase noise against offset frequency.

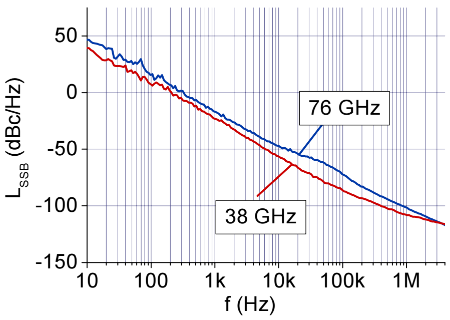

Fig. 6. Comparison of phase-noise for fundamental and second harmonic at V_d = 10 V.

Fig. 6 presents the results. Comparing the curves for the two harmonics one observes that the bump is present only for the second harmonic. Over a wide frequency range, the difference Δ_{LSSB} between the two curves is about 6 dB. This suggests that for the W-band measurement the Gunn-oscillator phase-noise is dominant. Therefore, the measured value of -102 dBc/Hz at 75 GHz represents an upper limit, which may include noise contributions from the downconversion source with the actual value being even lower.

In Fig. 7 a comparison of several published MMIC VCOs regarding the phase noise at an offset frequency of 1 MHz is shown. As stated above, for HBT technology no material system seems to be privileged for low phase-noise VCO applications. Therefore maximization of the loaded Q_L as shown in this paper seems to be the promising way for phase-noise reduction.

VI. CONCLUSION

A W-band MMIC oscillator based on GaInP/GaAs HBTs is presented. It yields excellent phase noise values of -102 dBc/Hz at 1 MHz offset and a large tuning bandwidth of 5 %. The design of the fundamental oscillator was optimized for highest loaded Q_L of the loop-gain. To our knowledge this is the first MMIC VCO in W band with phase-noise below -100 dBc/Hz at 1 MHz offset frequency.

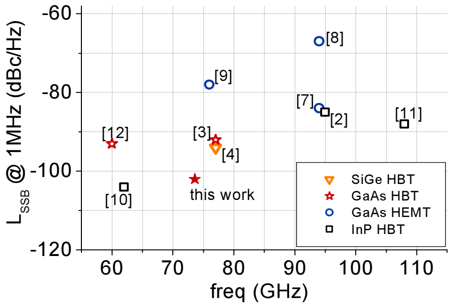

Fig. 7. Comparison of published phase-noise data for MMIC VCOs at 1 MHz offset frequency.

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