A 40 Gbps Broadband Amplifier for Modulator-Driver Applications Using a GaAs HBT Technology

Chafik Meliani, Matthias Rudolph, Jochen Hilsenbeck, and Wolfgang Heinrich

Ferdinand-Braun-Institut für Hoechstfrequenztechnik (FBH), 12489 Berlin / Germany
Email: meliani@fbh-berlin.de

ABSTRACT. ***A broadband amplifier suitable for high-bitrate modulator driver applications is fabricated using a GaAs-HBT process with f_T and f_{max} of 45 and 170 GHz, respectively. The design takes optimum advantage of the available technology, to obtain a broadband gain of 12 dB and a 3dB cut-off-frequency of 24 GHz. A smooth decrease around fc is chosen in order to keep a positive gain value at higher frequencies and a relatively flat group delay, which is a key condition for the eye-diagram opening. This appears to be the best way to combine high bitrate signal amplification with sufficiently high output voltage for a relatively low f_T HBT technology, compared to others, as InP HEMT or GaAs pHEMT. According to the NRZ power spectra, 40 Gb/s signal amplification is possible with such characteristics since the smooth slope condition is fulfilled. Eye diagram measurements at 40 Gb/s with several input signal swings are presented. A 4 Vpp output well-opened 40 Gb/s eye diagram is obtained with a large signal gain of 12 dB. This is a promising result for 40 Gb/s modulator driver applications using low-cost standard technologies and an interesting performance in terms of a maximum broadband f_c to (f_T, f_{max}) ratio.***

I. INTRODUCTION

In optical communication systems, the targets for near-future amplifiers are twofold: On the one hand, higher bitrates and improved eye-diagram quality for systems at 40 Gbit/s and, on the other hand, the use of technologies with lower cost.

Satisfactory 40 Gbit/s amplification has already been obtained using very high f_T and f_{max} technologies such as GaAs pHEMTs [1], or those still under development as the InP HEMT [2] and HBT [3]. The challenge today is the realization of broadband-amplification building blocks, with relatively low complexity, and using low-cost technologies. Thus, interesting results using CMOS have already been reported [4], as well as 40 Gb/s chips realized in SiGe-HBT processes [5]. But despite their high cut-off frequencies and the necessary technology improvements, the Si technologies still suffer from important frequency limitations when driving large currents, restricting them to low output voltage swings. Broadband preamplifiers using GaAs-based HBT technology were presented as well. However, in order to achieve the necessary high f_T values, significant enhancements in the technology are necessary compared to common standard HBT technology, such as selective regrowth of the extrinsic base layer [6].

The work presented in this paper demonstrates feasibility of broadband amplifiers using a standard GaAs-HBT technology for high-voltage applications at 40 Gb/s. Since the HBT technology provides extremely high f_{max} values, we were able to achieve 24 GHz cutoff frequency with HBTs that have an f_T of 36 GHz at the relevant bias point, while keeping the capability to operate at high output voltages.

II. TECHNOLOGY

The HBT MMICs are fabricated on the FBH 4" process line with stepper lithography. The epitaxial layers are grown using Metalorganic Vapor-Phase Epitaxy (MOVPE). For further details see [7]. Excessively high f_{max} values (>170 GHz at $V_{CE'}$=3 V) are achieved compared to the industry-standard f_T values (45 GHz at $V_{CE'}$=3 V). While f_T is mainly determined by the layer structure, f_{max} can be increased by optimizing process technology. In our case, mainly base resistance R_B and base-collector capacitance C_{bc} are modified. R_B is reduced by smaller under-etching of the emitter metal, which is used as an etch mask, in order to decrease the distance between emitter and base metalization. He^+-implantation is applied for device-isolation. In order to reduce the extrinsic base-collector capacitance $C_{bc\text{-}ex}$, we introduce an additional He^+ implantation in the outer region of the base fingers. As a result, the base layer below and the upper part of the collector (approx. 800 nm) become insulating, which strongly reduces $C_{bc\text{-}ex}$.

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Together with a reduction of the base-emitter distance from 1.3 µm to 0.5 µm, these process optimizations increased f_{max} from 95 GHz to 170 GHz.

IV. CIRCUIT DESIGN

The FBH HBT model [8,9] employed supports partition of intrinsic and extrinsic base-collector diode, non-ideal base currents, self-heating, base-emitter and base-collector break-down, current-dependence of base-collector capacitance $C_{bc,intr}$ and collector transit time τ_c. In order to include the thermal interaction between different emitter fingers inside a multi-finger power cell, the model was extended with regard to the thermal subcircuit. An additional thermal port allows to account for mutual and self-heating of each finger by a thermal resistance matrix.

The schematic diagram of the circuit is shown in Fig. 1. It consists of a five cascode-cell distributed amplifier, which provides wide bandwidth and good isolation by canceling the Miller effect.

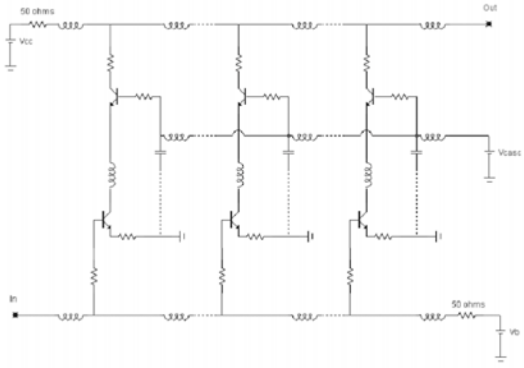

Figure 1. Schematic diagram of the distributed amplifier

According to the principle of distributed amplification, equivalent transmission lines are formed using either input or output active device capacitances plus coplanar lines for the inductive part. These artificial input and output lines are calculated to have 50 Ohm characteristic impedances and to achieve equal and flat group delay.

The collector line is terminated by a 50 Ohm load, which is designed in such a way that it provides DC bias power without significant thermal effects. The backward waves on the input transmission line are absorbed in the 50 Ohm resistor, which also feeds the transistors' base bias. The ground areas are interconnected along the transmission lines and around discontinuities to suppress parasitic modes and to ensure correct ground-current flowing path.

Two main problems exist for broadband-amplifier design, the gain-frequency slope and the gain ripple.

The first one is mainly solved by the unit-cell design: due to the very high HBT gain at low frequencies, an emitter feedback resistor of 20 Ohms was added to control the slope of the gain over the bandwidth. Moreover, the decoupling of the second cascode base represents a key condition for high-frequency operation. In our design, the base is locally decoupled with a series dump resistor of few Ohms and 5 pF capacitor to the nearest emitter, and is then connected to a longer DC bias line. Thus, floating ground planes due to the dimensions of the circuit will not influence the performances of the amplifier. However, this node has been carefully simulated because it can cause the real part of the output impedance to become negative, which can lead to instability if it is too sharply decoupled. Moreover, in this case, the gain decreases abruptly beyond the cut-off-frequency, what we don´t aim to. By the mean of supplementary resistors added on the artificial transmission lines and the feedback resistor on the emitter, a Bessel-like smooth decreasing slope gain has been optimised to keep a low variation of the group delay, and a significant gain, even beyond cut-off-frequency.

The second problem, the gain ripple, was solved by carefully optimizing the coplanar transmission lines for good matching while maintaining a low variation of the group delay and a smooth decrease of S_{21} at high frequencies. Fig. 2 presents the chip photo.

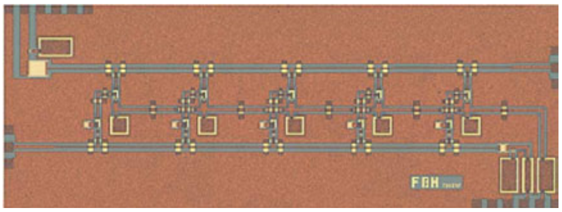

Fig. 2. Chip photo.

V. EXPERIMENTAL RESULTS

On-wafer small signal measurements show 12 dB broadband gain with a smooth continuous decrease up to a 3 dB cut-off-frequency of 24 GHz and keeps then an interesting gain beyond it. On the one hand to amplify the higher frequency components. On the other hand to have a smooth decrease in the time delay, to improve the waveform. DC consumption of the circuit is about 1400 mW for a 110 mA DC current and about 7 V collector voltage. Input and output matching is better than -5 dB within the bandwidth. Under these measurement conditions, the f_T of the transistor was 36 GHz. (S-parameters measurements in Fig. 3). The f_c to f_T ratio is of 66%. This is already interesting, but even higher values can be obtained with our technology and with similar topologies because of the high f_{max} to f_T ratio, by modifying the peaking effects and the impedances of the artificial transmission lines. But this degrades considerably the group delay.

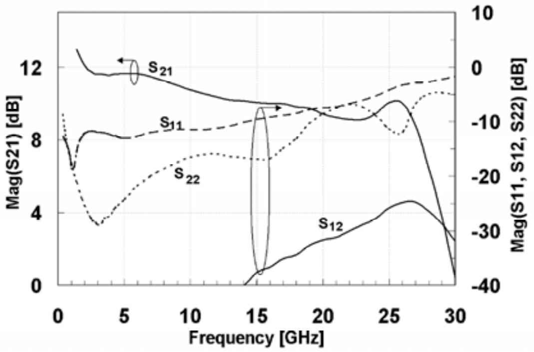

Figure 3. Measured S parameters

The large-signal behavior was tested with a 2^{31}-1 PRBS NRZ bit pattern provided by a 2:1 multiplexer. An attenuator was needed between the MUX and the amplifier so that the input signal swing reached approximately 500 mVpp.

Fig. 4 shows the measured input and output accumulated eye diagrams at 40 Gb/s. The circuit delivers an output signal amplitude of 2 Vpp with a well-opened eye diagram, at a large-signal gain of approximately 12 dB.

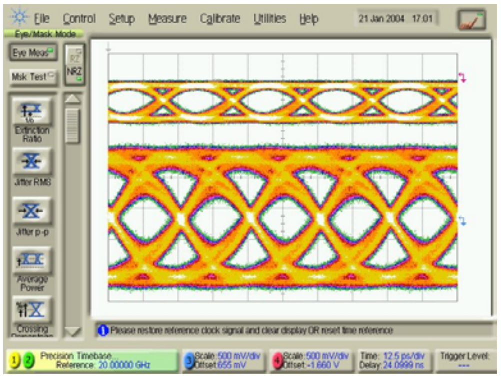

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Fig. 4. 2 Vpp output 40 Gb/s eye diagram(bottom) for 500 mVpp input signal (top). (500 mV/Div).

Fig. 5 presents the circuit eye diagrams at 40 Gb/s for a 1 Vpp input signal amplitude. A well opened eye diagram with 4 Vpp swing is obtained. Because of the shape of its spectra, the major part of the energy of a NRZ signal is contained in its first lobe. This explains that a correctly opened eye diagram at 40 Gb/s can be obtained with a -3dB cut-off-frequency f_c around 30 GHz, but only for smooth decreasing gain slope, thus keeping an useful high frequency gain available. Of course, higher f_c would yield better amplification of the higher frequency components, which would further improve the waveform and, consequently, the bit-error rate. But this is also due to the higher 3 dB-cut-off frequency in this case, which shifts the group delay bandwidth limit to higher frequencies, thus postponing the moment where the group delay starts to increase sharply. Because of this drastic increase of the group delay, for such an ultra-flat gain amplifier, f_c must be much higher than for flat group delay ones.

The Bessel-like gain type amplifier described in this paper produces the same effect by absorbing this group delay sharp variation around the –3 dB cut-off-frequency. This means that for a given bitrate signal, f_c can be much lower than in the case of the flat-gain amplifier, and is thus mainly limited by the necessity to amplify some part of the energy transmitted by the signal. In the case of the NRZ signal, around the upper limit of the first energy lobe. For our technology, this seems to be the best compromise to combine high frequency operation, high output voltage and high gain.

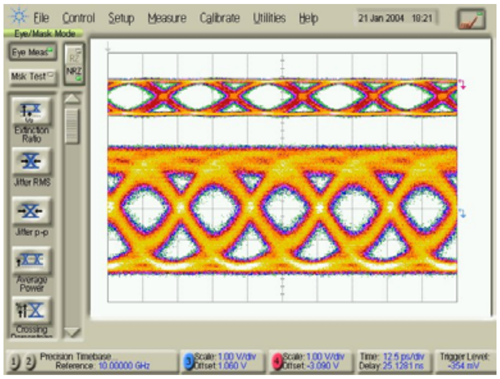

Fig. 5. 4 Vpp output 40 Gb/s eye diagram (bottom) for a 1 Vpp input signal (top). (1 V/Div).

VI. CONCLUSIONS

A broadband amplifier suitable for high bit-rate modulator drivers using a standard GaAs HBT technology is presented. Measured results demonstrate baseband operation with a -3dB cut-off-frequency of 24 GHz, with a smoothly decreasing broadband gain of 12 dB. This appears to be the best compromise to combine high bitrate signal amplification with sufficiently high output voltage for a relatively low f_T HBT technology compared to others as InP HEMT or GaAs pHEMT. At 40Gb/s, output voltage swings up to 4 Vpp at 50 Ω are achieved, with well-opened eye diagrams. Such a high output voltage swing, achieved using a standard GaAs technology with conventional stepper lithography, is a promising result for the low-cost technologies in 40 Gb/s modulator driver applications.

VII. ACKNOWLEDGEMENTS

The authors are grateful to M. Ludwig and M. Schlechtweg of the Fraunhofer Institut IAF, Freiburg, Germany, for performing the eye-diagram measurements, and to S. Schulz of FBH for performing the S-parameter measurements. This work is supported by the German BMBF under contract No. 01BP285.

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