120 GHz Broadband Chip-Interconnects for High Bit-Rate Communication Systems

M. Kunze[1], P. Talukder[1], F.J. Schmückle[1], W. Heinrich[1], D. Ferling[2], and K. Adam[2]

[1]Ferdinand-Braun-Institut (FBH), D-12489 Berlin / Germany
[2]ALCATEL, D-70435 Stuttgart / Germany

***Abstract* — A broad-band transition from a coaxial line to a CPW chip is simulated and realized. It is part of a 80 Gbps optoelectronic communication system covering the frequency range up to 120 GHz. The extremely large bandwidth require efforts not only to keep reflections low but also to suppress unwanted modes.**

I. Introduction

With increasing bit rates in optoelectronic communication systems, proper interconnects are to be realized in order to connect the chip to the outer world. To tackle the very high speed data exchange, a broad-band approach is inevitable providing low reflections and insertion loss as well as high immunity to package resonances. For 40 Gbps applications, the well-known approaches using BGA's, vias or bond wires result in a sufficient transmission behavior [1-4]. For higher frequencies, BGA arrays cannot be arranged dense enough and the bond wire inductance is prohibitively large. Other methods [5] use coaxial-to-microstrip transitions with SMA connectors, which are a method of choice for 10 Gbps applications but not applicable beyond 25 GHz.

In our work, the frequency range up to 120 GHz is covered. This demands the connecting elements between coaxial line and CPW on the chip to be small in size and to show only low discontinuity effects. The design of such a transition requires a thorough investigation of the dimensions and material properties of the CPW chip, the transition and the carrier substrate. The main task is to achieve a transition from coaxial mode into CPW mode with low insertion loss and reflections, while the parasitic modes generated are suppressed as much as possible.

This paper presents a detailed investigation on the transition, its electromagnetic properties, and the optimization concept. The results are verified by measurements.

II. The Structural Overview

Fig. 1 shows the CPW-to-coax transition. The interconnect is realized by so-called pre-shaped metal lids (PSLs), which consist of 15 µm thick Au and are bonded onto the metalizations of the chip and the coaxial line. At the end section of the coaxial line, the upper part is removed to allow proper mounting of the PSL (see Fig. 1). On the chip side, both InP and ceramics are used as substrate.

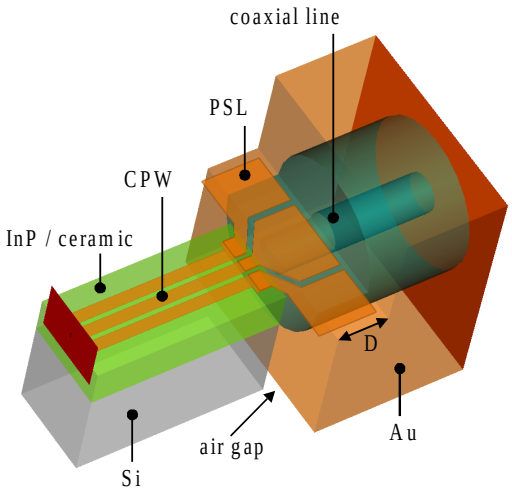

Fig. 1 The transition from a coaxial line to a CPW chip using a PSL. Along a length D, the upper half of the coaxial line is removed.

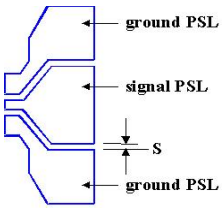

Fig. 2 Top view of the PSL. S denotes the separation between the ground and signal PSL

For the chip substrates, thicknesses from 250 µm to 620 µm are considered. To keep the interconnects short, the chip must be aligned in height with the coaxial core. Therefore, the chip is mounted onto a supporting carrier.

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In order to minimize influence of substrate moding by PPL modes, low-resitivity Silicon is used for the carrier.

For the dielectric of the coaxial line, we use Teflon. At the connecting end, the upper half of the coaxial line is cut away and a PSL (see Fig. 2) is bonded on both, core and boundary of the coaxial line and the chip, thus bridging the air gap. The diameter and dielectric of the coaxial line are chosen in such a way that the cutoff frequency of the first higher coaxial mode is beyond 110 GHz. The whole circuitry is embedded in a metal housing.

III. The Modes on the Chip Side

The chip cross-section forms a conductor-backed CPW and thus supports also parasitic parallel-plate-modes (PPL) [6], which propagate between the CPW chip surface and the backside metalization. Due to the broad frequency band up to 120 GHz, even higher-order modes can appear (though not propagate) at the upper end of the frequency range.

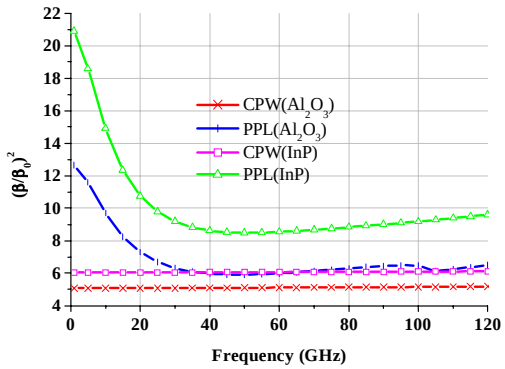

Fig. 3 Effective relative dielectric constant of CPW and PPL modes as a function of frequency and different substrate materials (250 µm InP-chip on 620 µm Si carrier (ρ = 4Ωcm) and 254 µm Al_2O_3 chip on 620 µm Si carrier ((ρ = 4Ωcm)).

The excitation of the PPL mode is enhanced by the radial field of the coaxial line within the cutted segment, where a large part of the electrical field points in a vertical direction as does the PPL mode on the chip side. To avoid coupling effects by the PPL mode, it is necessary to attenuate the PPL as much as possible. Therefore, simulations were carried out for various layer thicknesses (including a chip thickness variation) and material properties of the carrier.

The effective permittivity of the CPW and PPL modes is plotted in Fig. 3 for InP- and Al_2O_3 chips with Si carrier (ρ = 4Ωcm). Fig. 4 presents attenuation for an InP chip substrate with varying resistivity of the Si carrier. As one can see the attenuation of the PPL mode depends strongly on the resistivity of the Si carrier. Whereas the attenuation of the CPW mode is below 0.01 dB/mm at 120 GHz, the attenuation of the PPL mode covers the range up to 10 dB/mm. This is due to substrate losses in the Si.

Varying its resistivity, PPL attenuation shows a maximum. In case of high resistive Si, the PPL fields propagate almost unattenuated through the Si carrier. In the low-resistivity case, on the other hand, the PPL modes propagate also nearly unattenuated through the chip (Si acts nearly as electric wall).

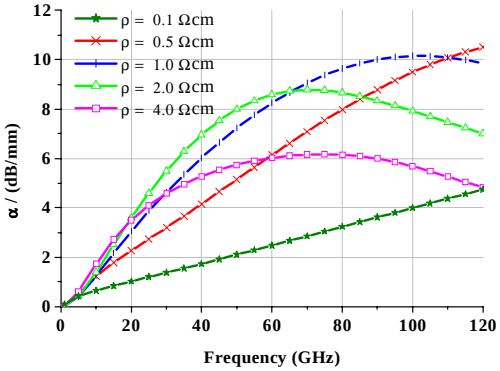

Fig. 4 PPL attenuation against frequency for InP chip and different carrier resistivities (250 µm InP chip on 620 µm Si carrier).

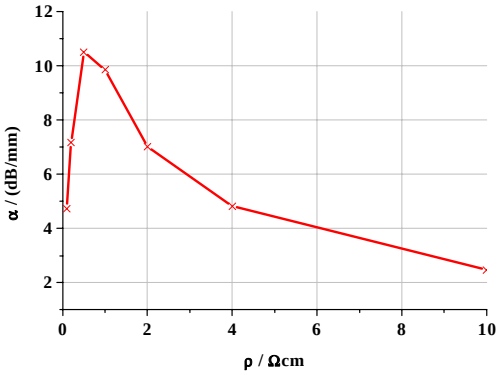

Fig. 5 PPL attenuation for varying resisitivity of the Si carrier at 120 GHz (250 µm InP chip on 620 µm Si).

From this behavior, it is clear that there must be a maximum in PPL attenuation corresponding to the resistivity of the Si carrier. In our case, for the chip and carrier dimensions and materials the maximum of PPL attenuation at 120 GHz is reached for resistivities ρ = 0.5 … 1.0 Ωcm (see Fig. 5).

IV. Interconnect Behavior

The key part of the interconnect are the PSLs. Fig. 2 illustrates the shape of the PSL. Their dimensions can be varied in optimizing the design. Of course, technological constraints and tolerances have to be considered (e.g., the gap (S) between signal and ground cannot be less than 10 µm). As a result, an external compensation structure could be avoided, so that the broadband performance was not affected. The em simulations were performed by means of CST Microwave Studio (FDTD) and an in-house FDFD software. Additional to the single interconnect, the back-to-back structure shown in Fig. 6 was analyzed to include coupling effects.

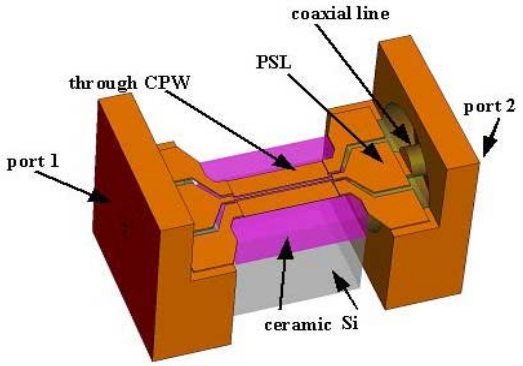

Fig. 6 Back-to-back structure of two coaxial-CPW interconnects according to Fig. 1 with thru-line on the chip.

Regarding the high-frequency characteristics, various parameters show a strong influence on reflection. E.g. the gap (S in fig. 2) between signal and ground PSL affects reflection rather strongly. For a range of the gap from 20 µm to 30 µm with an optimized value of 25 µm, the reflection coefficient differs by 6..7 dB. Another example is depicted in Fig. 7, which shows the influence of PSL metal thickness. Thus, also thickness of the PSL is a quantity to be accounted for in optimization.

A further sensitive parameter is the length of the cutting section of the coaxial line (D in Fig. 1), which should be on the one hand as small as possible but, on the other hand, needs a certain length to allow for proper PSL bonding. The designed length of the cutting section is 350 µm and allows for a 50 µm tolerance.

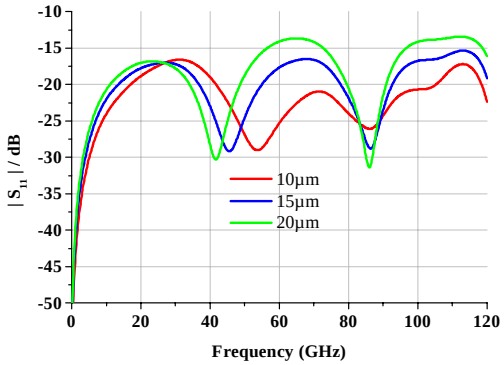

Fig. 7 Influence of the PSL thickness: reflection coefficient of the back-to-back structure against frequency.

Particularly critical, however, is the air gap (100 µm) between substrate and coax, which is difficult to control during manufacturing.

Besides the interconnect behavior, isolation needs to be assessed. For this purpose, the back-to-back structure in Fig. 6 is employed replacing the thru-line by two opposite shorted CPW stubs on the chip. Fig. 8 shows simulated isolation for an InP chip and different Si carrier thicknesses. As can be seen, the thicker Si carrier improves isolation. This is a result of the increase in PPL attenuation (see Sec. II).

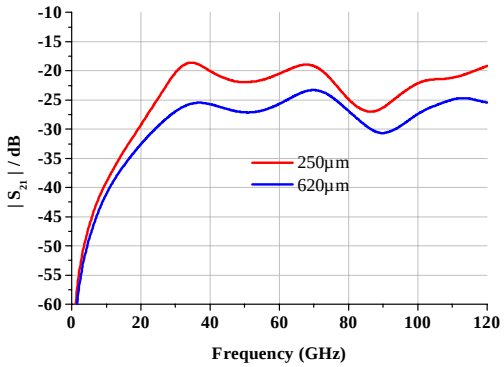

Fig. 8 Isolation of CPW lines in the back-to-back structure (comparable to Fig. 6, but with shorted stubs on the CPW chip) for different thicknesses of the Si carrier and a InP chip of 250 µm thickness.

With the optimized transition, a test set-up was fabricated (see Fig. 9) using a 1mm long CPW thru-line on the chip. The whole transition is embedded in a metal housing as shown in Fig. 10.

Fig. 9 Photograph of the test set-up with PSLs in the center (top and bottom).

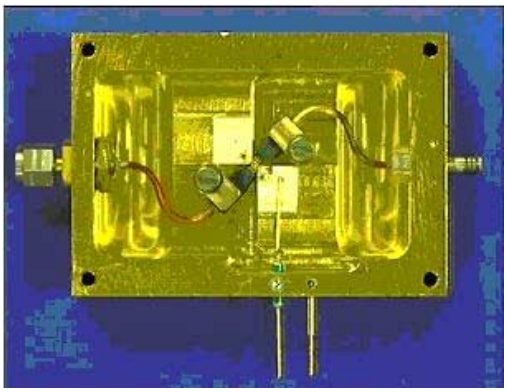

Fig. 10 Test fixture with embedded test chip.

Fig. 11 presents the measurement results. The ripples in the measurements are due to the length of the coaxial connecting lines in the package. The results show a good agreement up to 120 GHz. Reflection is lower than -10 dB for the back-to-back structure over the entire frequency range, what means that the single transition has a reflection better than –16 dB. The measurements include the reflections due to the coaxial connectors (1 mm type) on both sides. The deviations in transmission parameters ($|S_{21}|$) can be attributed to conductor loss, which is not accounted for in the simulations.

V. Conclusions

A coaxial-to-CPW transition for broadband applications up to 120 GHz is presented. Pre-shaped metal lids (PSLs) are used as connecting structure. The interconnect was optimized including fabrication tolerances, which represent a critical issue due to the high-frequency of operation. Special emphasis is on suppressing parasitic PPL modes in the substrate. The optimized transition provides good transmission behavior with less than –16 dB measured reflection for a single interconnect.

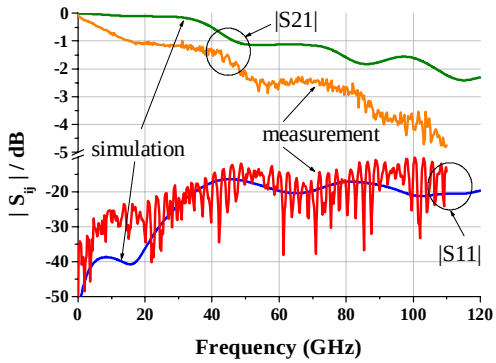

Fig. 11 Reflection and transmission parameters against frequency: Simulation and measurement data of the back-to-back structure with 1 mm long through CPW line on an Al_2O_3 chip.

Acknowledgements

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