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Integrated Circuits and 3D-Packaging for Low-Power 24 GHz Front End

ntegrierte Schaltungen und 3D-Aufbautechnik für energiesparende 24-GHz-Front-Ends

Abstract
Design and experimental results for a low-power monolithic 24 GHz front end are described. As basic circuits, VCO and mixer are presented. The circuits are realized on GaAs using heterobipolar transistors. The VCO reaches 19 % efficiency at 4.3 dBm output power and 14.5 mW DC power consumption. The circuits are to be integrated together with a special slot antenna using flip-chip technology. Simulation data on this novel antenna approach demonstrate acceptable gain characteristics around 3 dB, despite of its small size.

Übersicht
Der Beitrag beschreibt Simulationen und experimentelle Resultate zu einem monolithischen Frontend bei 24 GHz mit minimiertem Energieverbrauch. Als Grundschaltungen werden Ergebnisse zu VCO und Mischer vorgestellt, die auf GaAs mit Heterobipolartransistoren realisiert werden. Der VCO erreicht einen Wirkungsgrad von 19 % bei 4.3 dBm Ausgangsleistung und 14.5 mW Leistungsverbrauch. Die Schaltungen sollen zusammen mit einer neuartigen Schlitzantenne integriert werden, die mit Hilfe der Flip-Chip-Technologie realisiert wird. Die Simulationsergebnisse zeigen trotz der Miniaturisierung einen akzeptablen Gewinn um 3 dB.

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Für die Dokumentation
Millimeterwellenfrontend / VCO / Mischer / Schlitzantenne / Integration

1. Introduction

One of the special features investigated in the framework of the AVM project is to exploit space diversity for the wireless communication between the egrains. This means that antennas with a certain directivity must be employed, which, in turn requires antenna dimensions to be in the order of or larger than the wavelength. Since, on the other hand, egrain size is to be kept as small as possible, the tradeoff between antenna directivity and egrain dimensions determines the frequency of operation for the communication link. For an egrain dimension of 1 cm, one ends up with frequencies in the 30 GHz range or beyond. Taking into account spectrum allocation and front-end technologies available, the ISM band at 24.5 GHz turns out to be the most interesting choice balancing the different specifications and constraints. Therefore, the front end has to operate in the 24.5 GHz ISM band.

Regarding the key circuits, any front-end architecture needs a VCO as local oscillator and a mixer for down and up-conversion. Therefore, in the following sections, examples for these two circuit types are treated. Common about them is the demand for low DC power consumption. Because the antenna is to be integrated with the circuits, a lossless semiconductor substrate must be used. Hence, we apply a GaAs-based HBT MMIC process. In comparison to HEMT technology, the HBT version offers lower $1/f$ noise and thus better phase-noise performance, which is beneficial for the VCO.

The paper is organized as follows: Sec. 2 provides data on the HBT process, while Sec. 3presents the status in VCO and mixer development. Section 4 then describes the slot antenna, which can be integrated together with the circuits in a sandwich-type of 3D structure.

2. The GaAs Technology Used

The circuits as well as the passive antenna structure are realized applying an InGaP/GaAs HBT integrated-circuit process. The HBT epitaxial-layer structures are grown by means of Metal Organic Vapor-Phase Epitaxy (MOVPE). A β_{max}/R_{SBI}-ratio of 0.5 $(\Omega/sq)^{-1}$ is achieved indicating the very good quality of the epitaxial material. The HBT MMICs are fabricated at the FBH using an industry-compatible 4" process line with stepper lithography. In total, 14 lithography levels are needed for the MMIC process (see [1]).

In order to achieve a maximum frequency of oscillation f_{max} , both the base resistance R_B and the total base-collector capacitance $C_{BC,intr} + C_{EX}$ (see **Fig. 1a**) are minimized. In the first case, a reduction of the total base resistance R_B (i.e., $R_{CB} + R_{B2}$) of 47 % is achieved by downscaling the emitter-base finger distance d_{EB} from 1.3 µm to 0.5 µm. Thus, f_{max} was increased from 95 to 150 GHz (f_T = 40 GHz). Regarding the capacitance $C_{BC,intr} + C_{EX}$,

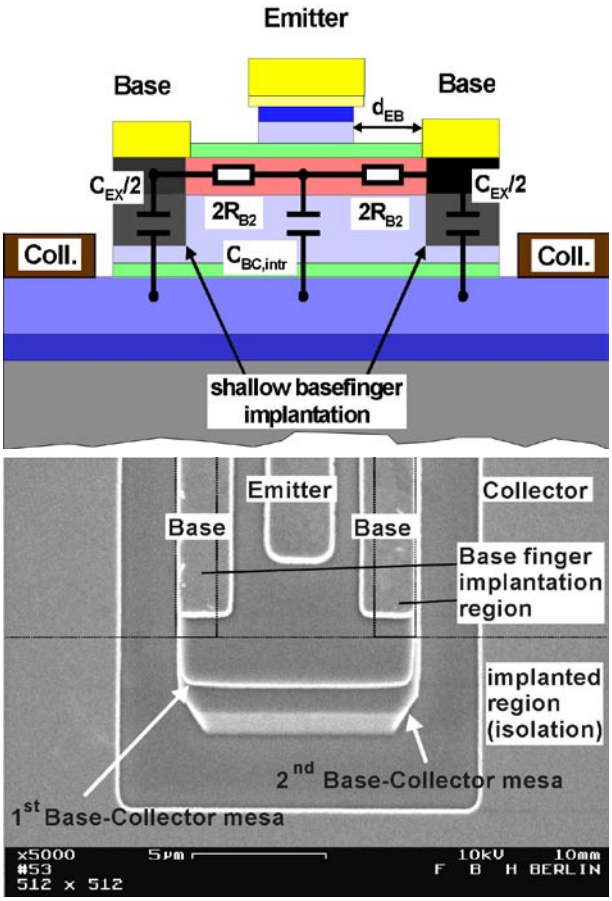

Fig. 1: The process: GaAs/GaInP-HBT after collector metalization: a) cross section and b) SEM image

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the extrinsic base-collector-capacitance C_{EX} is reduced by introducing a shallow base-finger implantation in the outer region of the base fingers. In this way, both the parasitic layer of the base region and almost 80 % of the collector in the outer base finger area are isolated (**Fig. 1**). From small-signal equivalent-circuit extractions, we observe a reduction of ($C_{BC,intr}$ + C_{EX}) by 44 %. As a result, in combination with a down-scaled d_{EB}, f_{max} is further increased to 170 GHz. Thus, with f_T = 40 GHz we achieve a record high f_{max}/f_T ratio of 4.25. These transit frequencies provide enough of gain margin for operation at 24 GHz.

Regarding the passive elements, MIM capacitors (dielectric material: SiN_x), thin film resistors (NiCr), spiral inductors, coplanar waveguides, and air bridges (electroplated Au) are available in the process. As an example, **Fig. 2** shows a detailed SEM image of a broadband amplifier with a 1 × 2 × 10-μm^2-HBT as the active device.

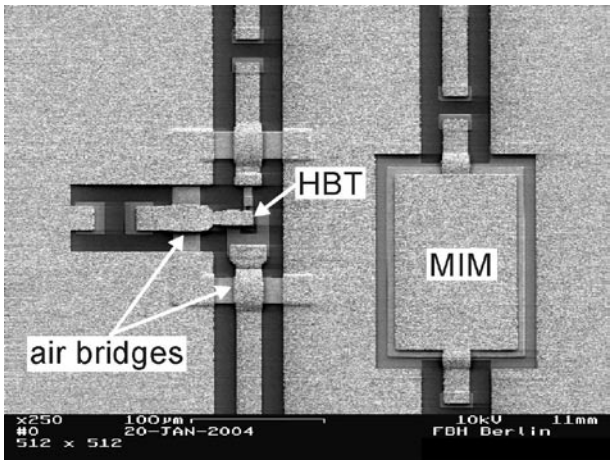

Fig. 2: MMIC detail: broadband amplifier with a 1 × 2 × 10-μm^2 GaAs/GaInP-HBT, airbridges, and a MIM capacitor (process status after bridge technology)

3. The Circuits

3.1 Voltage-controlled oscillator (VCO)

The VCO is the core part of the front-end system and a key building block for higher-level functions. For our specific application, it will be used either as a local oscillator for the mixer function, which needs a relatively low output power level, or as an emitting signal generator, where a higher output power is required. The first conclusions concerning the oscillator features are: it should deliver a few dBm (up to 6) of output power at a DC consumption below 10 mW. This corresponds to a power efficiency between 5 and 40 % for the worst-case scenario. In the 20 .... 30 GHz band, however, such values have not yet been reported in the literature. The relevant efficiencies are still below the 10 % limit [2].

From the circuit-design point of view, the high efficiency value required leads to some decisions regarding the oscillator concept: First, based on our experience with previous designs (e. g. [3]), single transistor oscillators are clearly preferred. A push-push or differential configuration is beneficial for the phase-noise characteristics, but much more critical in terms of energy balance. Second, the question arises whether the desired output-power can be directly taken from a single-transistor oscillator, while keeping the DC consumption low enough, or whether it is better to add an amplifier stage to an oscillator with low output power but high efficiency.

When arguing only from an efficiency point of view, the second configuration is clearly the best, because the efficiency potential of narrow-band amplifiers is significantly higher than that of oscillators. But, when combining the constraints of low power and very high frequency, many of the respective amplifier concepts become difficult or even impossible to realize. If the VCO-with-amplifier architecture is applied, the output power of the oscillation stage must be very low, which contradicts the input-power requirements of large-signal amplifier topologies such as class C or class E. However, other classes, such as class AB, can be interesting for these applications.

All in all, there is no clear a-priori answer to the question of the oscillator configuration. It strongly depends on the possible efficiencies and power consumptions of the oscillation stages. Thus, the first step in circuit design is to investigate, within the framework of GaAs HBT technology, several oscillator topologies regarding their capabilities for low-power high-efficiency operation. This is described in the following.

Oscillator Concept

The oscillators are based on a single-transistor feedback structure [4]. The inductors at base and collector make the transistor unstable and the capacitive loading on the emitter is designed to fulfill the phase condition (see schematic diagram in **Fig. 3**).

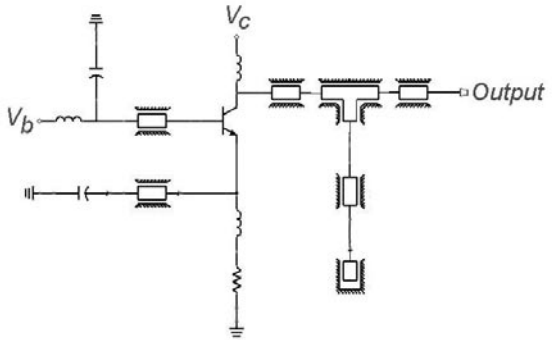

Fig. 3: Schematics of the oscillator

In our case, and in addition to its classical function for the impedance matching, the collector stub is also used to fix the output power level extracted from the collector by changing the impedance value seen by the transistor. These inductive elements are responsible for the steepness of the phase condition and consequently for the phase-noise performance. Regarding the phase noise, a larger transistor contributes lower 1/*f* noise, but, unfortunately, at the expense of a higher bias current and thus increased DC consumption.

The Low-Power Issue

As described above, the first optimization regarding power is the use of single-transistor oscillator topologies. Nevertheless, these topologies have to be adapted by avoiding any unnecessary passive power consumption in the biasing and feedback parts. Also, the initial bias conditions of the transistor determine the operation class of the circuit. Due to the fact that the small-signal gain must be larger than unity to initiate oscillations and that the amplified signal amplitudes are low, the transistor must be biased to have a non-zero initial loop gain, which rules out class C or class B operation, for example. For these large-signal amplifying topologies, the transistor does not show small-signal gain, which is required to start the oscillation. Instead, class A is the most intuitive choice for an oscillator. Simply, a part of the output signal is injected via the small-signal loop gain into the input to maintain oscillation. However, class A clearly does not optimize efficiency, because the small signal loop gain does not systematically increase when the operating point power is increased. Thus, the tradeoff between high frequency and high efficiency led us to apply class AB.

In this kind of topology, the transistor consumes very low power because it is biased at the limit of the saturation region, but, on

the other hand, has enough gain to initiate oscillation. When the steady state is reached, the mean DC current is slightly higher than the initial value, but still remains acceptable in terms of efficiency. Thus, the design is as simple and clear as class A, while efficiency is enhanced, even for very low DC consumption.

The Circuits Realized

Based on these considerations, we realized two oscillator designs, one using a $3 \times 30\ \mu m^2$ and the other a $2 \times 10\ \mu m^2$ emitter-area transistor (see **Fig. 4**).

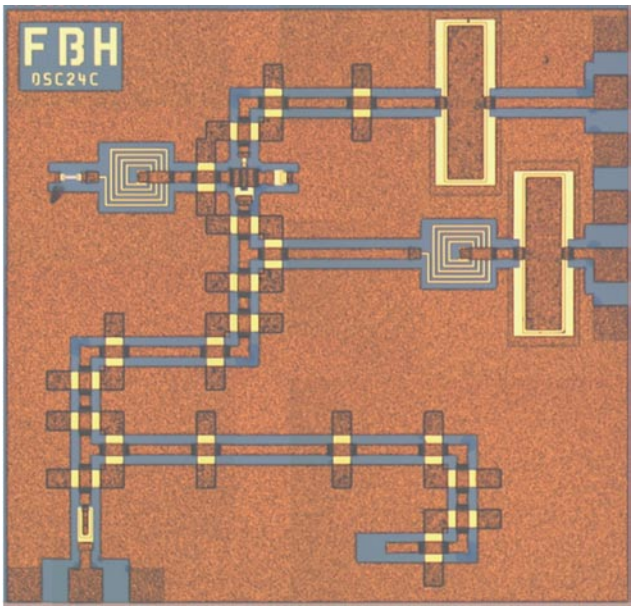

Fig. 4: Chip photo of the VCO

Both circuits are operated in class AB and follow the series-feedback single-transistor concept (see Fig. 3). Applying a smaller transistor allows to decrease the value of bias collector-current from 20 mA to a more realistic 3 mA value, following our simulations based on the HBT model according to [5]. In this way, we obtain a much lower DC consumption without drastically decreasing the output power. The design is implemented using subsequently S-parameters simulation to optimize loop gain and phase condition as well as harmonic-balance simulations to optimize the power. Good agreement between simulations and measurements is obtained.

Fig. 5 shows the output power of the two oscillators at 24 GHz as a function of DC consumption for all circuits on a wafer.

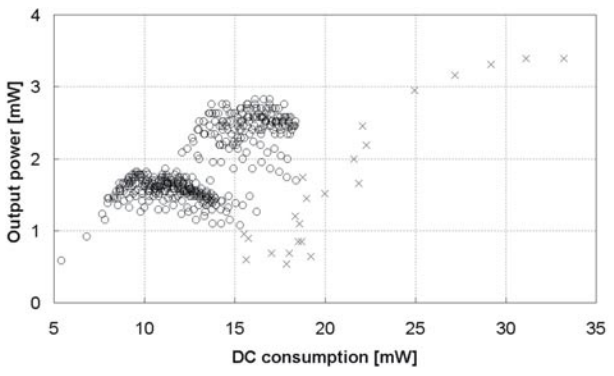

Fig. 5: Output power against DC power consumption for different supply voltage and bias conditions
(circuits with $2 \times 10\ \mu m^2$ (o) and $3 \times 30\ \mu m^2$ (x) transistors; wafer mapping based on spectrum-analyzer measurements)

An automated mapping procedure using a spectrum analyzer is applied, which causes some scattering of data due to measurement uncertainties but provides the full picture of all circuits on the wafer. The results plotted in Fig. 5 clearly prove that the DC consumption is lowered very much when reducing the transistor size while the output power is kept in the same range. While an output power of 1 mW requires up to 20 mW of DC input power for the larger-transistor version, the same RF power is obtained at only 10 mW DC consumption for the smaller transistor. With this circuit version, 4 dBm output power are obtained realizing an efficiency of 19 %. These are record values for such a high frequency (24 GHz) and such a low absolute value of DC consumption (14.5 mW).

The trade-off when further decreasing transistor size will be between the gain and the extrinsic parasitic elements of the transistor. In our case, this limit is not yet reached. Nevertheless, one must notice that the DC power does not exactly scale with transistor size, as could be expected from a simplified model. This is due to power absorption in the parasitic elements, which does not contribute to RF output and the relative amount of which grows with decreasing transistor size.

The phase noise for the two circuit versions was measured applying an EE5504 Agilent system, according to the delay-line method. **Fig. 6** provides the phase noise data of the two circuits versus the offset frequency. At 100 kHz offset frequency, we obtain SSB values of –64 dBc/Hz and –72 dBc/Hz for the smaller and the larger transistor version, respectively.

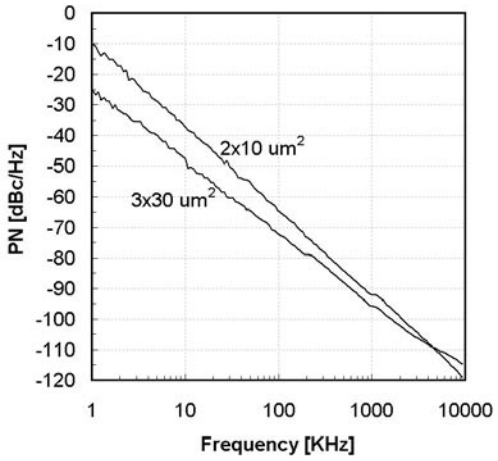

Fig. 6: SSB phase noise PN as a function of offset frequency for the two VCO versions

Summarizing one can state that the oscillator performance achieved is promising in terms of the intended system specs. Furthermore, we can expect that the lower limit of transistor size is not yet reached, and, thus, the DC power consumption can be further reduced. Phase noise values are already within the acceptable range, but some improvements are possible to realize. There is, however, a certain trade-off between efficiency and phase noise.

3.2 Mixer

As for the oscillator, the limited power budget puts severe constraints on the mixer as well. Most mixer topologies found in literature for K Band are Schottky-diode mixers [6, 7] or resistive mixers [8]. Among many advantages, these topologies always introduce losses, which would make an additional amplifier necessary. Due to the overall power budget this is not reasonable. Therefore, an active mixer topology is chosen, which provides enough gain so that a separate preamplifier in the receiver branch can be avoided. Cascode mixers can be found realized with FET

devices up to V band [9], still providing conversion gain. Basically, cascode mixers are always part of a Gilbert cell [10] but not balancing all inputs and output.

For a first design, an unbalanced homodyne mixer is to be realized. **Fig. 7** illustrates the layout.

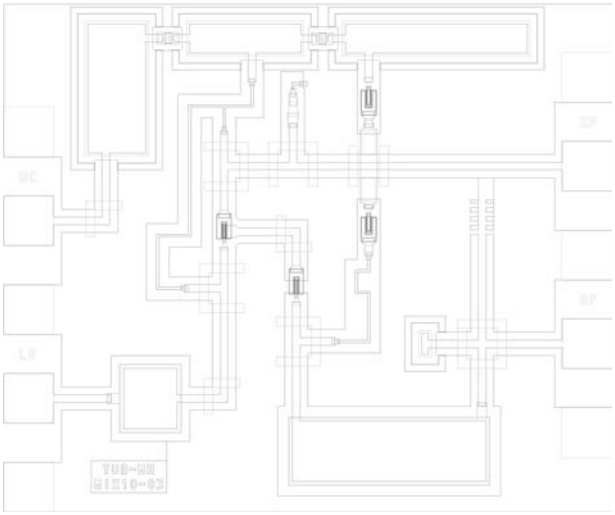

Fig. 7: Layout of a homodyne mixer

Using 3 × 30 µm transistors, a down-converter with a current consumption of a few mA at the given supply voltage of 3 V is designed. A load of 1 kOhm is used to model the input of the subsequent high-impedance baseband stage. Simulations show the following characteristics: A local oscillator power of 4 dBm is sufficient for satisfactory operation. Conversion gain reaches almost 6 dB, with a 1 dB gain compression at –15 dBm input power.

Circuits like this mixer tend to be unstable in many cases. Because very small transistors are used, stability can be reached with a slight modification. In our case, a series capacitor-resistor configuration parallel to the load ensures overall stability of the circuit. Further structures with even smaller transistors even may not need any additional elements to provide stability, which in any case introduce losses. If smaller transistors are used with the same collector current, current density is increased, which leads to improved mixing performance.

In order to demonstrate operation of the front end, a 2.45 GHz transceiver IC will be employed for baseband processing. Hence, the heterodyne mixer has to be designed for an intermediate frequency of 2.45 GHz. This circuit is shown in **Fig. 8**. Transistor size in this case is 2 × 10 um.

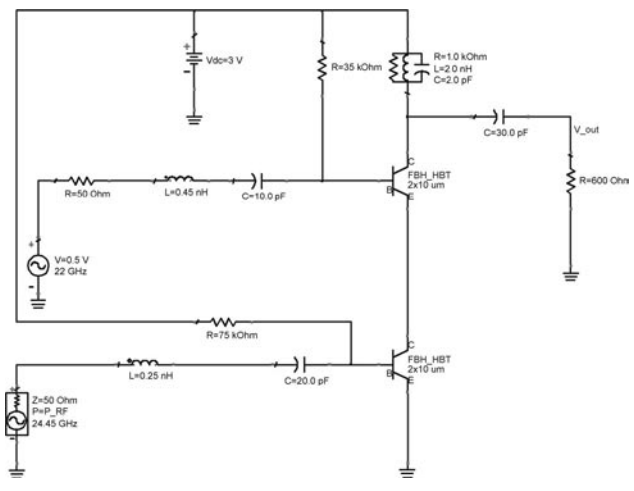

Fig. 8: Schematics of a heterodyne mixer with IF at 2.45 GHz

Basis currents can also be generated by replacing the high resistances by a series diode-resistor topology. There will be always a constant voltage drop over the diode, so the resistors can be chosen much smaller to achieve the desired bias voltage. **Fig. 9** shows simulated conversion gain as a function of RF input power for various voltages of oscillator (LO) output. The LO output is modeled as a voltage source with an internal resistor of 50 Ohms. According to the simulations, a conversion gain of more than 8 dB is achieved with 0.5 V oscillator input voltage, which corresponds to 4 dBm LO input power. A gain compression better than –15 dBm is obtained.

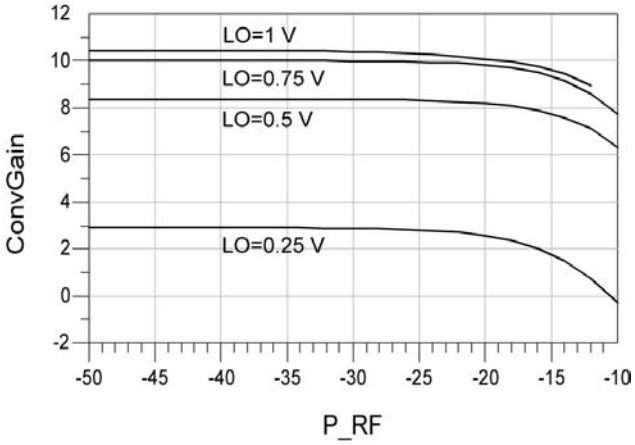

Fig. 9: Conversion Gain as a function of RF input power for different RF voltages at the local oscillator (LO) input (simulation data)

Focus of our further work will be to reduce battery current in the heterodyne example. Presently, current consumption is 2 mA applying a 3 V source. Furthermore, an important detail in order to achieve high conversion gain is the band-stop filter in the DC path. To this end, a higher-order filter can increase mixer performance, which will be an additional subject of future work.

4. 3D Slot Antenna

Using flip-chip technology, a novel type of a slot antenna is developed, which can be integrated together with the circuits and leads to a 3D sandwich assembly. **Fig. 10** presents a schematic view of the antenna.

It is composed of two 500 µm thick GaAs substrates with 3 µm thick metalization on the front-side, which are backside-mounted on a metal block (more precisely, this block may contain arbitrary material, it is sufficient if the side walls are shielding). In our case, the block is assumed to be 2.5 mm thick. In the GaAs substrate, via fences act as shielding side walls. The two mounted

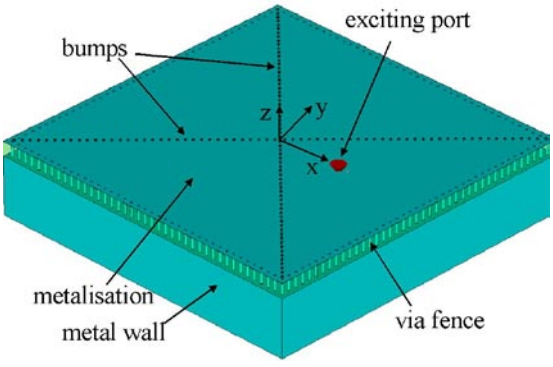

Fig. 10: Schematic view of the sandwich structure with the parallel-plate antenna section in the center

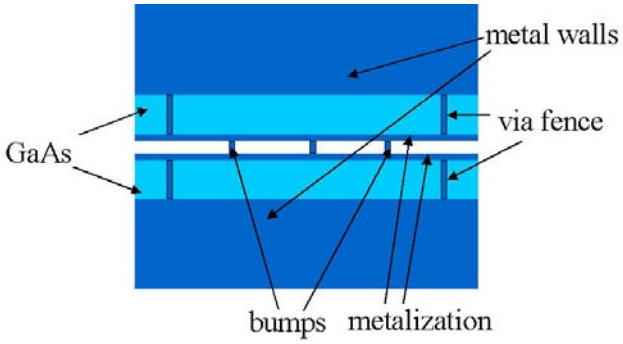

Fig. 11: Structure in Fig. 10: Cross-section of the antenna plane Diagonal bump rows act as separating walls. The antennas are excited by a discrete port between the parallel plates. The via fences in the GaAs substrate along the four sides form shielding walls

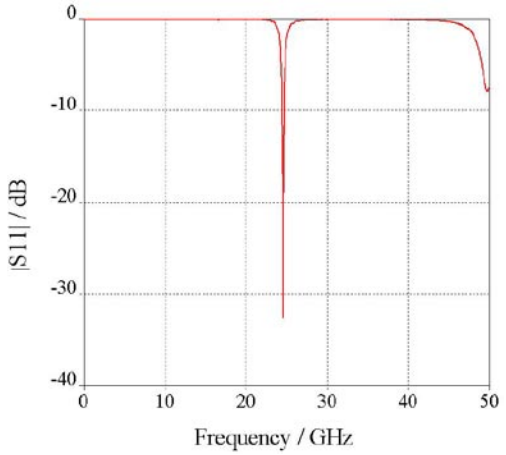

Fig. 12: Magnitude of reflection coefficient of the discrete exciting port vs. frequency
(simulation data; resonance at 24.5 GHz with very steep slopes)

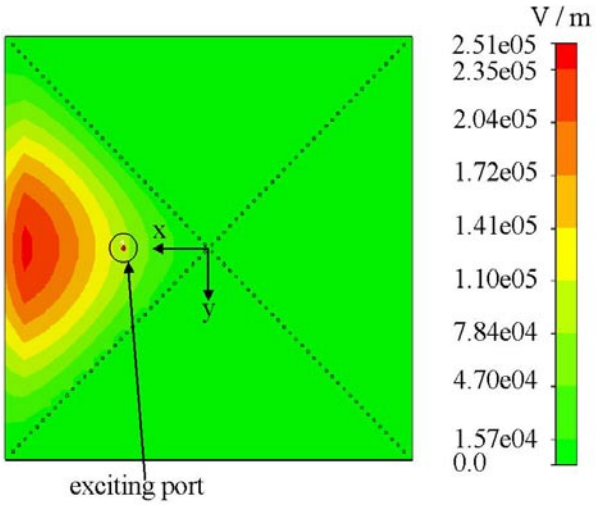

Fig. 13: Electric field distribution in the *x*-*y* plane at 24.5 GHz within the cavity
(*z* =0, see Fig. 11).

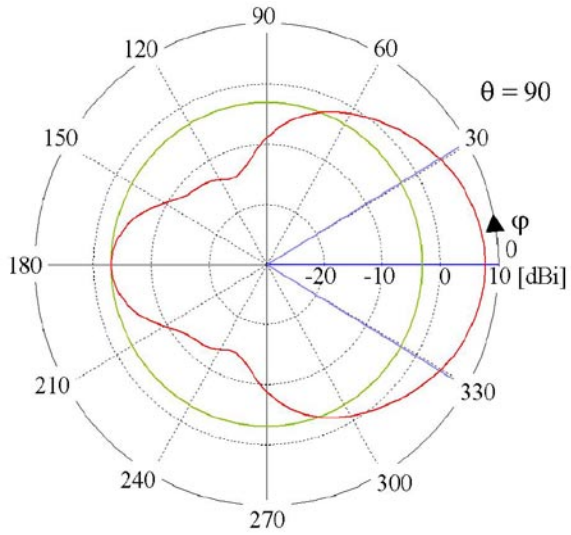

Fig. 14: Simulated radiation pattern in dBi as a function of φ at $\theta = 90°$
(frequency 24.5 GHz, main-lobe magnitude 7.6 dBi, main-lobe direction $\varphi = 0°$, angular width in φ (3 dB): 62°, side-lobe level -11 dBi).

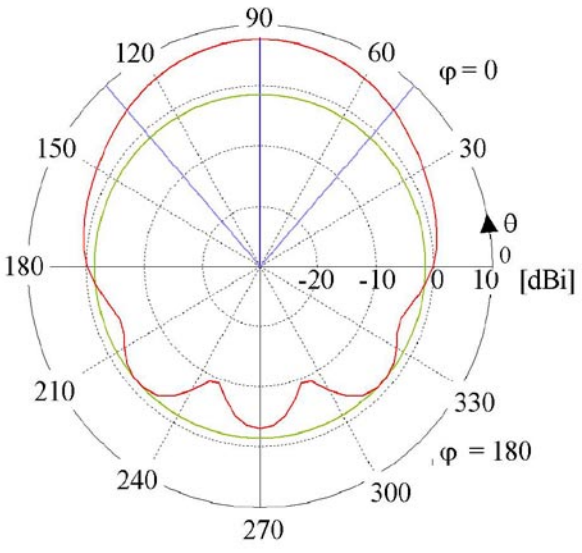

Fig. 15: Simulated radiation pattern in dBi as a function of θ at $\varphi = 0°$ and 180°, respectively
(frequency 24.5 GHz, main-lobe magnitude 7.6 dBi, main-lobe direction in $\theta = 90°$, angular width in θ (3 dB): 83°, side-lobe level –9 dBi)

substrates are then flip-chip soldered face-to-face using bumps of 80 µm diameter and height in between. The resulting sandwich structure forms a cube with a slot antenna on each side.

Fig. 11 shows a cross-sectional view of the antenna part of the structure in Fig. 10. The coordinate system is chosen such that the metalization on the GaAs substrates is oriented in *x*-*y* direction and the height dimension of the bumps is aligned with the z-axis, with the origin centered. The whole structure is of square type with a dimension of 12 mm.

In order to allow for space diversity, bump fences are placed along the diagonals of the square. Placing the bumps this way creates four sectoral horn antennas, the inner sides of which are formed by bump walls. Since the bumps are only 80 µm high, the openings of the horns form a wide thin slot with an extremely large aspect ratio of 150. Therefore, its radiation characteristics resemble that of a slot more than the typical horn antenna pattern. Each antenna is excited by a separate feeding bump. In the final structure, the circuits are to be located next to this bump, which avoids unnecessary long and lossy interconnects between ICs and antenna.

As the characteristic impedance of the parallel-plate structure between the metalizations is low due to the high aspect ratio, the antennas are highly resonant ones. Thus, each of the four antenna sections can be thought of as a cavity resonator, the open sides of which can be approximated by magnetic walls. The resonance frequency depends mainly on the diagonal dimension of the cavity resonator (i.e., the side length of the cube structure is equal to $\lambda/2$) and the matching at resonance depends on the position of the feeding source within the resonator.

The entire four-sector antenna structure was simulated by a 3D electromagnetic field simulator (Microwave Studio by CST). One

of the four cavities is excited (see Figs. 11 and 13). The structure with a dimension of 12 mm is designed to operate in resonance at 24.5 GHz, the intended frequency of operation. In **Fig. 12**, the resulting input reflection at the excitation port is plotted against frequency with 50 ohms reference impedance.

One recognizes good matching at 24.5 GHz and steep slopes off the resonance frequency. This is an interesting feature of the antenna, which acts both as antenna and as a filter. In other words, one does not require a separate input or output filter for the front end. **Fig. 13** visualizes the electric field distribution in the excited cavity. As can be expected, the field intensity is maximum at the center of the edges of the structure and fades out at the corners.

Fig. 14 depicts the simulated far-field pattern of the antenna in the θ plane (θ denotes the angle referred to the z axis) when varying φ (the angle in the x-y plane with $\varphi = 0$ identical to the x axis). Accordingly, **Fig. 15** shows the far-field pattern in the φ plane for different values of θ. It is clear from these two curves that the main lobe (7.6 dBi) of the radiation pattern is in the direction of the sector excited, i.e., at $\theta = 90°$ and $\varphi = 0°$, and the side lobes (–9 dBi maximum) are low compared to the main lobe.

An antenna directivity of 7.6 dBi is achieved. Preliminary simulations taking into account the conductor losses indicate that efficiency does not decrease below 50 %. Thus, an antenna gain around 3.5 dB is expected, which is excellent given the overall antenna size, which is only about half a free-space wavelength.

5. Conclusions

The results prove that using transistors with small emitter area together with a suitable circuit concept allows to realize low-power 24 GHz VCOs and mixer circuits on GaAs. Furthermore, a novel slot-antenna approach is presented, which can be integrated with the circuits and allows space-diversity applications. Flip-chip technology is used for the 3D mounting and assembly. The VCO achieves a record 19% efficiency at 4.3 dBm output power. For 3 V bias, this results in currents in the 10 mA range for the RF-to-IF chain and offers interesting properties for all types of portable wireless communication and sensor systems. Operating them in the 24 GHz range allows to take advantage of moderate antenna gain while maintaining low power consumption.

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