Thin Film Integration of Passives – Single Components, Filters, Integrated Passive Devices

Kai Zoschke, Jürgen Wolf, Michael Töpper, Oswin Ehrmann, Thomas Fritzsch, Katrin Scherpinski, Herbert Reichl
Franz-Josef Schmückle[1]
Fraunhofer Institute for Reliability and Microintegration, Berlin
Gustav-Meyer-Allee 25, 13355 Berlin, Germany
kai.zoschke@izm.fraunhofer.de
[1]Ferdinand-Braun-Institut für Höchstfrequenztechnik
Albert-Einstein-Straße 11, 12489 Berlin, Germany

Abstract

The increasing demands on future electronic products require more efficient system integration technologies. Especially the package density gap at board level with the high integrated circuits (ICs) on the one and the discrete passive components on the other hand has to be closed by new packaging technologies which integrate the passive components into the substrate, an interposer or the IC itself.

This paper presents investigations for the common integration of inductors, resistors, capacitors as well as passive filter structures in a thin film build up based on copper and Benzocyclobutene (BCB). Technologies from wafer level packaging were adapted for manufacturing of the integrated components.

The examinations were carried out with special focus on integrated coils and passive filter structures. Build up, design, processing as well as results of the electrical characterization of the integrated components are described in detail. Furthermore an integrated passive device (IPD) for application as filter element in the Bluetooth band is presented.

1. Introduction

Today most of the passive components required in an electronic system are assembled as discrete components or passive arrays. Such components offer broad value ranges for all passive types as well as tight tolerances and availability in different package sizes. But in relation to an IC with a very high integration density a discrete passive component requires a lot of space for the realization of its single inductive, capacitive or resistive function. For systems with a high number of passives this can lead to an additional need for board area comparable to the area consumed by the active devices. But beside the additional area consumption aspects like parasitic influences, caused by long feedings and solder connections, reduced assembly yield caused by many additional solder joints as well as high assembly costs caused by high placement times can be disadvantageous for the realization of future electronic systems. [1, 2, 3, 4]

Especially products in the “hand held” as well as in the “high performance” sector are indicated to be affected by these disadvantages. Thus these products are the driving force for new technologies overcoming the drawbacks of discrete passives.

One promising way, which is presented in this work, is the integration of passive components into thin film multi layer systems. With this approach multi chip module substrates (MCM-D) or integrated passive devices (IPDs) can be realized with passive elements having high accuracy and high density.

For answering general questions regarding design as well as the technological realization of integrated passive structures a feasibility study was carried out using a simple thin film build up suitable for the integration of inductors, resistors and capacitors. Since design parameters for resistors and capacitors can be easily calculated in this first approach the different influences of the coils’ design parameters on their electrical behavior were investigated. Furthermore passive filter structures for 2.4GHz were realized to examine their electrical performance. For predicting the final filter behavior as close as possible detailed electrical models were established including parasitic influences caused by the elements and transmission lines.

In the second phase of this work, a first application of the collected results, a flip chip mountable integrated passive device was realized for application as filter circuit in the Bluetooth frequency band.

2. Thin film build up and single passive elements

Figure 1 shows the thin film build up used for the integration of inductors, resistors and capacitors. This build up was derived from the demands of all three passive types.

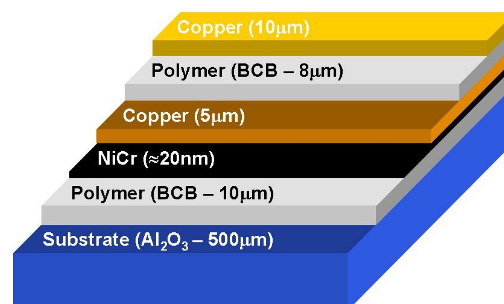


Figure 1: Thin film build up for production of integrated passive components

Since each additional layer means additional mask steps and thus additional costs, planar spirals are the preferable structures for the realization of integrated inductors in thin film technology. With this approach only two metal layers are needed. In one of them a conductor is formed to a spiral to

achieve a strong magnetic field coupling. In case of a single layer coil (fig. 2/1) the other metal layer is used to route the inner coil contact to the outside by using a simple underpass. In case of a double layer coil (fig. 2/2) the underpass is replaced by additional windings. In order to reach high quality factors electroplated copper with a thickness of 5µm for the first and 10µm for the second metal layer was chosen. To prevent substrate losses, ceramic (Al_2O_3) instead of silicon was chosen. Consequently, a planarization layer has to be applied to smooth the relatively rough surface of the ceramic material [5].

Since two metal layers are required for coil realization anyway, integrated capacitors can be realized with parallel plate structures (fig. 2/3). If, like in this case, no additional dielectric material is applied the interlayer polymer has to be used as dielectric for the capacitors. For reaching high capacitance values the interlayer dielectric has to be as thin as possible. But at the same time it has to be thick enough to provide good planarization and insulation properties for the lower metal layer. Because of its good planarization properties photostructurable Benzocyclobutene (Cyclotene from Dow Chemical) was chosen as interlayer dielectric [6, 7]. A thickness of 8µm Benzocycloutene (BCB) between metal layers was fixed as target value.

For the realization of integrated resistors an additional layer providing an adjustable sheet resistance, good patterning properties as well as a low temperature coefficient is necessary. Nickel Chromium (NiCr), which is one of the most successful resistor materials, was chosen. NiCr can be deposited by sputtering and structured by wet chemical etching. The sheet resistance of a NiCr layer can be adjusted between 10Ω/sq. and 100Ω/sq. by different deposition times [8]. Since resistor values are strongly influenced by the waviness of the underground the resistors are realized as first structures directly onto the planarization layer (fig. 2/4).

Furthermore transmission lines are required to enable impedance controlled connections between certain elements. With the given build up both micro strip lines as well as coplanar wave guides can be realized.

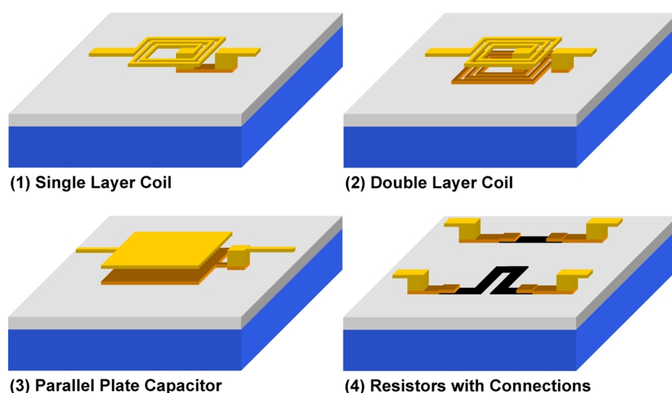


Figure 2: Single elements which can be realized in the given build up

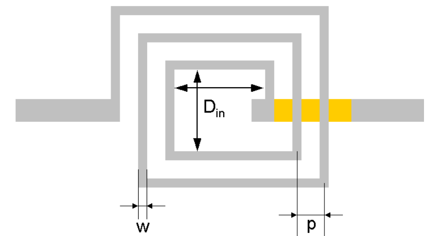
3. Design of the passive components

3.1 Inductor design

Planar thin film inductors have a lot of different design parameters which are form of the spiral (square, octagonal, Archimedes), number of layers, number of turns, coil area, line width, line pitch as well as line thickness. Because of the large variety of possibilities the form was not altered in this work and fixed to the square type for all examined inductors. Figure 3 shows the design parameters for a square type coil with 2.5 turns.

Figure 3:

Square type coil with inner window length D_{in}, line pitch p and line width w



The designed coil collection includes coils with 1.5 to 5.5 turns in steps of 1 turn, each of them with inner window lengths from 100µm to 500µm in steps of 100µm. These 25 basic coils were designed with different line pitches p and line widths w of p=20µm / w=10µm, p=40µm / w=30µm as well as p=40µm / w=10µm, bringing the number to 75 coils. These 75 coils were realized in single and double layer fashion, bringing the total to 150 coils.

A strong increase in capacitance of double layer coils compared to single layer coils is reported in [9], mainly caused by their relatively low layer to layer distance. To diminish that increase the influence of layer shifting should be examined. Thus additional double layer coils were designed in which upper and lower spiral are shifted relative to each other by a quarter and a half pitch of the coils turns. Such shifts were only designed for the coils with 200µm inner window length and line widths of 10µm.

3.2 Filter design

Low pass, band pass as well as band stop filters with cut off and center frequencies of 2.4GHz were designed in micro strip fashion for the given build up. The band stop filters are Tschebyscheff filters of 6th and 10th order. The low pass filter is also a Tschebyscheff type of 9th order whereas the band pass is a Cauer filter.

As a first step of each filter design a realization concept was worked out fixing the element forms and arrangements as well as the length of the transmission lines connecting them.

In order to create electrical filter models which describe the integrated structures sufficiently it was necessary to consider the parasitic influences of the single elements by using electrical models describing their behavior. Since no detailed design library was available the single filter elements were simulated using a 3D FD simulation tool.

To prevent long iterative simulation cycles which can be time consuming the layout of each element was roughly calculated prior simulation to meet the elements target values as close as possible. For the rough calculation of the capacitors' geometries the formula for the ideal parallel plate capacitor was used with a dielectric constant ε_r=2,65 for BCB.

The approach for inductors' coarse calculation was derived from other examinations on square type inductors reporting a linear dependence of inductance from their inner window length [9, 10, 11]. Because of this the approximation in equation 1 was used to calculate the necessary inner window lengths $D_{in/wanted}$ for a target inductance L_{wanted} from a known inductance L_{known} with the inner diameter $D_{in/known}$.

The values indicated with "known" were taken from former examinations on single layer square type inductors integrated in a similar thin film build up with inner window lengths of 200µm, line pitches of 20µm and line widths of 10µm.

$$\frac{D_{in/wanted}}{D_{in/known}} = \frac{L_{wanted}}{L_{known}} \quad (eq.1)$$

After coarse calculation of the element layouts for each element a lossless 3D simulation was performed. With the simulation results a parameter extraction on suitable electrical models was carried out. The used equivalent circuit models for capacitors and inductors are shown in figure 4. The extracted and predicted values from rough calculation showed good correspondence. At this stage a first electrical model of the whole integrated filter structure was created. Thus the effects of the elements' parasitic influences on the filter performance could be determined. Effects were center or cut off frequency shifts to lower frequencies as well as distortions in the attenuation behavior of the filters. The frequency shifts could be compensated by adjusted element values, but the distortions could only be decreased.

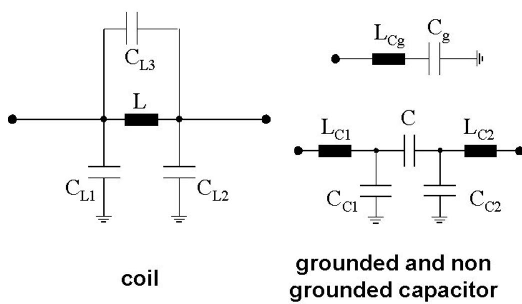


Figure 4: Equivalent circuit models for inductors and capacitors

To be able to consider the conductor influences the filter model was expanded by additional elements describing the conductor segments between the various elements. Therefore a micro strip line with an impedance of 50Ω was simulated for the given build up. The additional elements led to frequency shifts und could be compensated partly by lowering the values of the main elements.

At the last step the series resistances of the inductors, which were not considered up to this point, were estimated. Therefore the skin depth in copper at 2.4GHz was calculated using equation 2 with f=2.4GHz, $\kappa=58.14\cdot10^6$S/m, $\mu_0=1.256\cdot10^{-6}$Vs/Am and μ_r=1.

$$\delta = \frac{1}{\sqrt{\pi \cdot f \cdot \kappa \cdot \mu_0 \cdot \mu_r}} \quad (eq. \quad 2)$$

$$R_F = \frac{1}{\kappa \cdot \delta} \quad (eq.3)$$

$$R = R_F \cdot \frac{l_{Coil}}{u_{Cond}} \quad (eq.4)$$

With that skin depth the value of the coppers' specific surface resistance could be calculated using equation 3. Together with the ratio of the coils' conductor lengths l_{Coil} to the conductor circumference u_{Cond} the coils resistance at 2.4GHz could be calculated with equation 4.

But this calculation is only valid for smooth surfaces. According to [12], where the influences of surface roughness on eddy current losses are theoretically discussed, the calculated value of the coils resistance was multiplied by 1.2. After adding the resistances to the filter model a final simulation was performed.

Since the element values were altered during filter design the element layouts had to be adjusted. In cases of small adjustments the methods from rough calculation were used. Otherwise a new simulation was performed.

4. Process flow and process optimizations

4.1 Process flow

The process flow for the realization of the integrated passive components is shown in figure 5.

At first a 10µm thick BCB planarization layer is realized by spin coating and curing of the photosensitive Cyclotene 4026-46 from Dow Chemical. This layer is necessary to equalize defects and roughness of the substrate surface [5] (fig. 5/1). After BCB curing a NiCr layer is deposited by sputtering a target consisting of 50% Ni and 50% Cr. To define the resistor structures this layer is masked by a first photolithography step using AZ 4562 photo resist from Clariant (fig. 5/2). In a following step the masked layer is structured by wet chemical etching to create the wanted resistors. After etch mask removal a short oxygen plasma treatment in a reactive ion etcher is performed to remove resist residues from the surface (fig. 5/3).

In the next step a 100nm thick Ti:W adhesion layer followed by a 300nm thick copper seed layer is deposited by RF sputtering. After that the copper is masked by a photo resist (AZ 4562), to define the structures of the first metal layer (fig. 5/4). Then the metal structures are formed by electroplating of copper into the resist mask openings (fig. 5/5). After the deposition process the resist mask is stripped

and differential etching steps of the copper as well as the Ti:W layers are done. Finally, a short dry etch step in oxygen / SF6 plasma is performed to remove the upper layer of the BCB, which was interspersed with Ti:W during sputtering (fig. 5/6).

Now the interlayer polymer has to be realized. Therefore a spin coating process using the same BCB formulation as for the planarization layer is applied. After a soft bake the prepolymer is exposed (fig. 5/7) and developed using tank development to define the via holes connecting the two metal layers of the build up (fig. 5/8). After a short post bake step the polymer is cured. As final step a dry etch (descum) has to be carried out in oxygen / SF6 plasma. This plasma treatment removes BCB residues remaining in the vias after development.

For the realization of the second metal layer the same process steps as for the first one including sputtering of adhesion and seed layers, creation of resist mask (fig. 5/9), electroplating of metal structures (fig. 5/10) as well as resist removing and differential etching (fig. 5/11) are carried out.

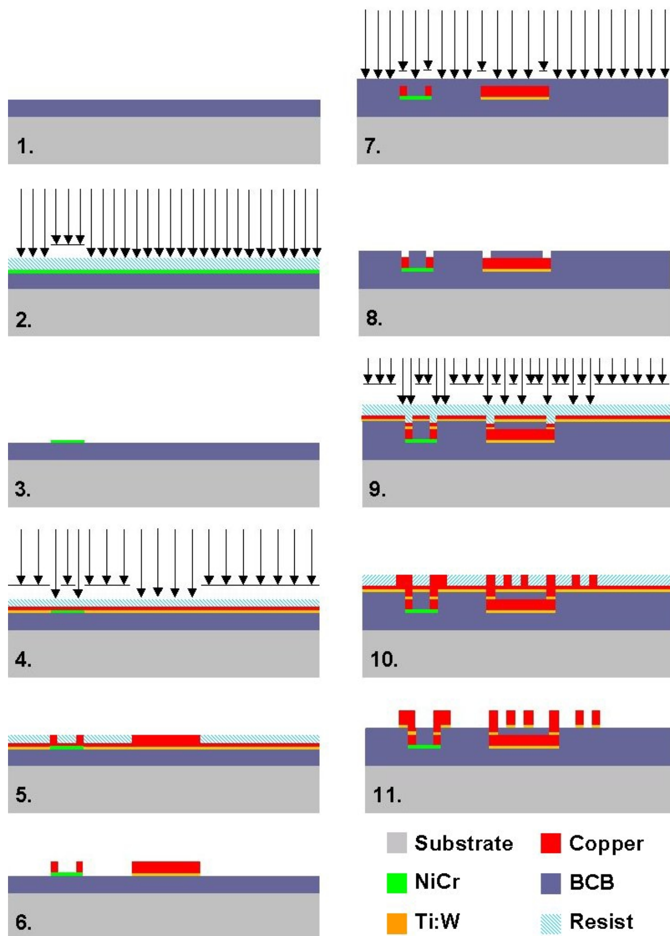


Figure 5: Process flow

4.2 Process optimizations

Some of the processes are critical regarding realization of certain element values and had to be optimized with separated trials. These critical processes are the deposition of a NiCr layer with a sheet resistance of 100Ω/sq. as well as the realization of a BCB interlayer thickness of nearly 8µm between first and second copper layer.

The spin speed for the deposition of the interlayer BCB was determined on separate test wafers, which were prepared to have the same structures in the first metal layer. The optimal spin on speed was found with 2200rpm using a closed cover spin box. After cure and descum a final interlayer BCB thickness between 7.5µm and 8.5µm was received.

The deposition tests for the NiCr layer were carried out on separate test wafers covered with a BCB planarization layer. Some processes between sputter deposition of the NiCr (fig. 5/2) and spin on of the interlayer BCB (fig. 5/7) were identified to increase the value of sheet resistance. In detail these process steps are:

- oxygen plasma treatment after removal of etch resist
- back sputtering prior deposition of the Ti:W
- treatment in oxygen / SF6 plasma after differential etching of the Ti:W adhesion layer

Taking into account these things the sheet resistance after NiCr sputtering has to be lower than 100Ω/sq. to be increased to 100Ω/sq. by the following steps. To optimize the sputter time several tests were performed. Wafers with unstructured NiCr layers were exposed to the three processes. After each step the sheet resistance was measured at 49 points per wafer. The result of the optimization is shown in figure 6. The diagram shows the mean values of sheet resistance for six wafers after sputtering as well as the increase of sheet resistance caused by the three process steps. Additionally the standard deviations of the sheet resistances for the six wafers are shown.

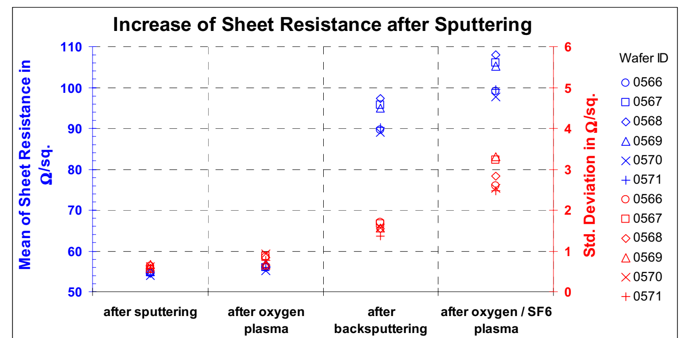


Figure 6: Increase of sheet resistance after sputtering

5. Results

5.1 Inductors

For inductor characterization at first the S-parameters of each coil were measured using a vector network analyzer. After that a parameter extraction was performed for each coil using the π-equivalent circuit model in figure 7. The inductance and series resistance of the coil are represented by L and R. The elements C_1 and C_2 describe the coil's capacitance to ground,

C_3 represents the inter-winding capacitance emerging between the coil's lines and layers.

Figure 7:

Equivalent circuit for inductor parameter extraction

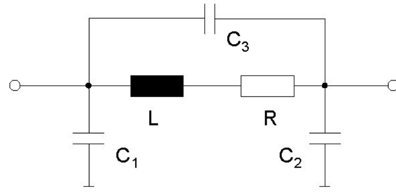


Figure 8 shows the inductance of single layer coils with line pitches of 20µm and line widths of 10µm as function of their turns N. The functions have the form of equation 5. The constant b has nearly same values of 1.72 for the different window lengths. The constant a rises from 0.3nH for 100µm window length to 1.79nH for 500µm window length.

$$L(N) = a \cdot N^b \quad (eq. 5)$$

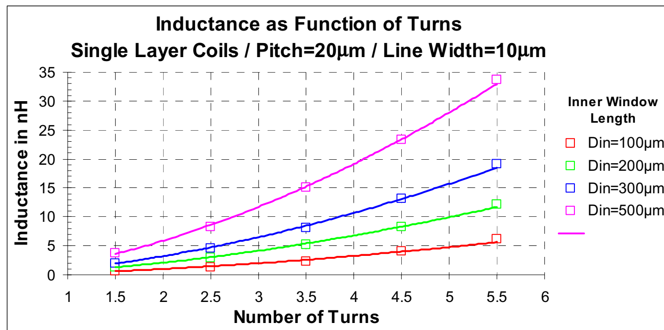


Figure 8: Inductance as function of turns

Figure 9 shows the inductance of single layer coils with line pitches of 20µm and line widths of 10µm as function of their inner window length D_{in}. The functions have the form of equation 6. The constant c rises from 0.0075nH/µm for 1.5 turns to 0.0693nH/µm for 5.5 turns. The constant d decreases form –0.16nH for 1.5 turns to –1.25nH for 5.5 turns.

$$L(D_{in}) = c \cdot D_{in} + d \quad (eq. 6)$$

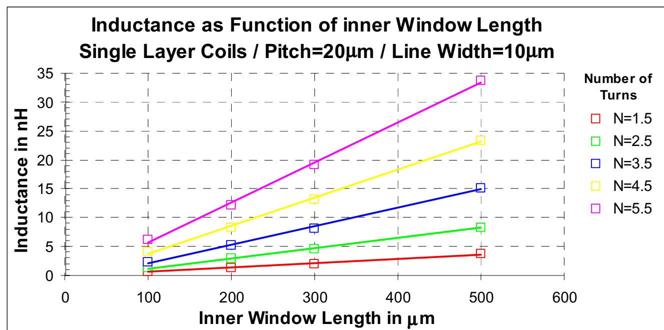


Figure 9: Inductance as function of inner window length

In quality the same dependencies were obtained for the comparable double layer coils but with steeper increases of inductance with number of turns as well as inner window length. Figure 10 shows the inductance ratio from comparable single and double layer coils. As can be seen in the diagram with double layer coils up to four times higher inductance values can be realized within the same area compared to single layer coils. Thus identical inductance values can be realized within smaller areas using double layer instead of single layer coils. This advantage in area saving is illustrated in figure 11 where the area required for double and single layer coils is shown as function of their inductance.

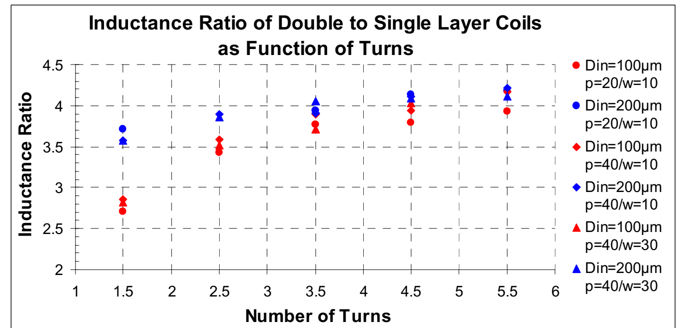


Figure 10: Inductance ratio between double and single layer coils

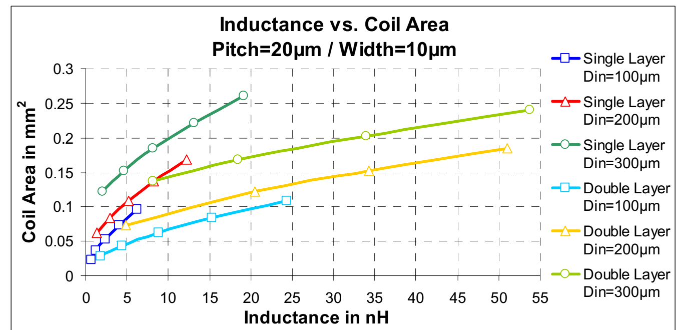


Figure 11: Foot print of single and double layer coils

But with regard to quality factors double layer coils cannot compete with single layer coils. Figure 12 shows a comparison of quality factors between single and double layer coils in the same inductance range. As can be seen the quality factor for single layer coils is always a bit higher. This can be explained by the higher resistance of the lower spiral of double layer coils, which has only a thickness of 5µm instead of 10µm.

In general single layer coils have quality factors between 30 and 40, whereas double layer coils only reach values below 25. Figure 13 shows typical curves for quality factor as function of frequency for single and double layer coils. The quality factors were directly calculated form the measured S parameters.

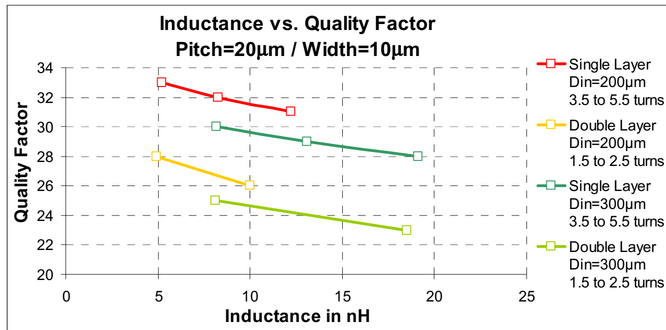


Figure 12: Quality factors of single and double layer coils of identical inductance ranges

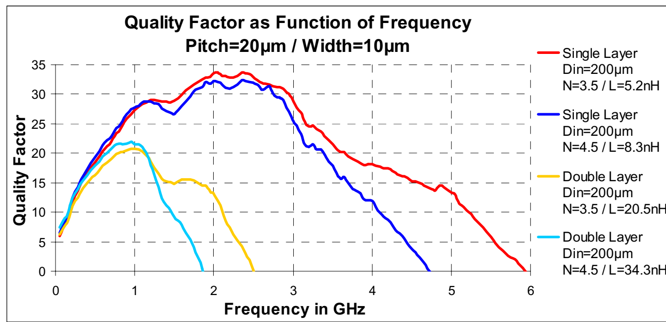


Figure 13: Quality factor of single and double layer coils as function of frequency

Another disadvantage of double layer coils is their high inter-winding capacitance (C_3 in figure 7) mainly caused by the small layer to layer distance. Since C_3 is directly parallel to the inductance the resonance frequency is strongly affected by this element. With the other elements from the equivalent circuit model the resonance frequency of the coils can be calculated by equation 7.

$$f_{res} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{1}{L \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2} + C_3 \right)} - \frac{R^2}{L^2}} \quad (eq.\ 7)$$

In figure 14 the calculated resonance frequencies of single and double layer coils are plotted against their inductance values. In the inductance ranges which can be realized by both coil types, the single layer is the better choice regarding resonance frequency.

For reaching higher resonance frequencies of double layer coils it is necessary to reduce their inter-winding capacitance. Such a reduction can be achieved by shifting the two spirals of double layer coils relative to each other as can be seen in figure 15. The diagram shows the ratio of inter-winding capacitance for double layer coils with and without layer shift s. S=0 means no shift. S=p/4 indicates a layer shift of a quarter of the pitch and s=p/2 a layer shift of half the pitch. As can be seen for a layer shift of half the pitch the inter winding capacitance can be reduced by half compared to the non shifted type. The influence of the reduced capacitance is shown in figure 16 were inductance is plotted against resonance frequency for double layer coils with and without layer shift. As predicted the reduced inter-winding capacitance of the double layer coils with layer shift leads to higher resonance frequencies.

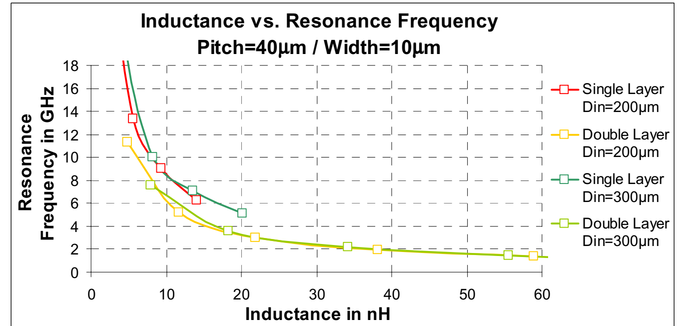


Figure 14: Inductance vs. Resonance Frequency for single and double layer coils

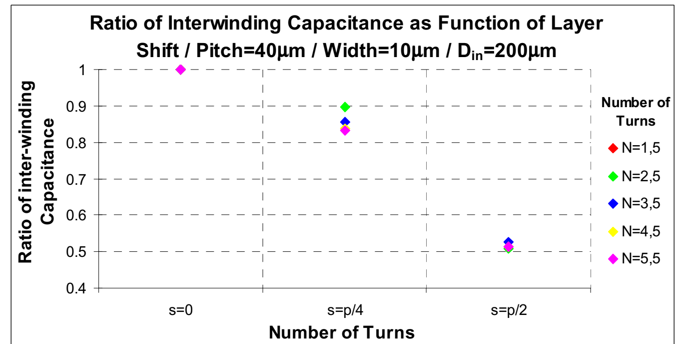


Figure 15: Influence of layer shift on inter winding capacitance

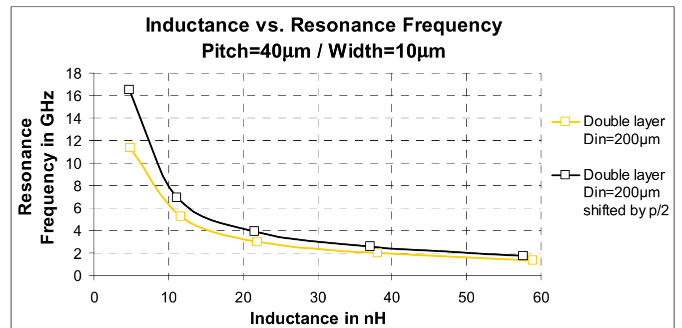


Figure 16: Influence of layer shift on resonance frequency

5.2 Filters

Figure 17 shows pictures of the realized filter structures. The filters include inductors with values between 2.3nH and 18nH and capacitors with values between 150fF and 1580fF. The band stop filter was realized in two types with 6 elements (band stop filter 1) as well as with 10 elements (band stop filter 2).

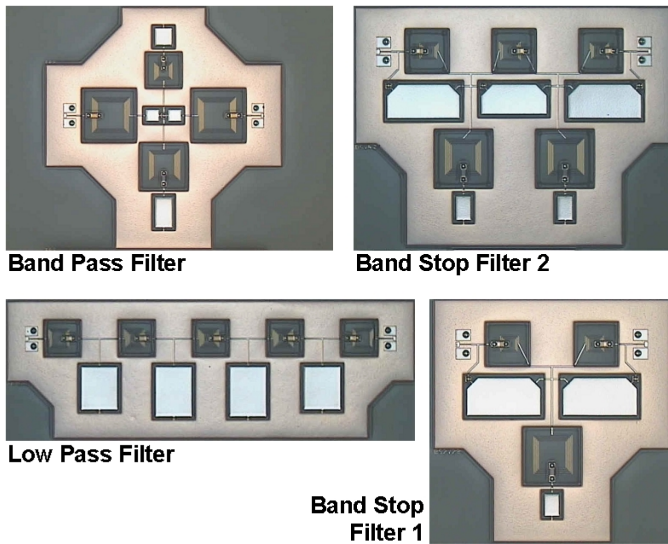


Figure 17: Realized integrated filters

Figures 18 to 21 show simulated and measured attenuations for the filters shown in figure 17. As can be seen from the diagrams a good fitting between measurement and simulation could be reached for all filter types indicating the correctness of the used models and calculations during the design phase. A very important factor for achieving these good results was the interlayer BCB thickness, which could be realized with high accuracy for a target value of 8µm.

The band pass filter (fig. 18) has a center frequency of 2.38GHz, a maximum insertion loss of –1.6dB and a band width of 600MHz.

The low pass filter (fig. 19) has a cut off frequency of 2,4GHz with –2.8dB. The insertion loss decreases strongly to –18,2dB at 2,8GHz.

The band stop filter 1 (fig. 20) has a center frequency of 2.38GHz and a band width of 600MHz. The minimum insertion loss is –33.6dB.

The band pass filter 2 (fig. 21) has a center frequency of 2.38GHz with a band width of 650MHz. The minimum insertion loss of this filter is –50.7dB.

These promising results show the feasibility for the integration of passive filters using thin film technologies.

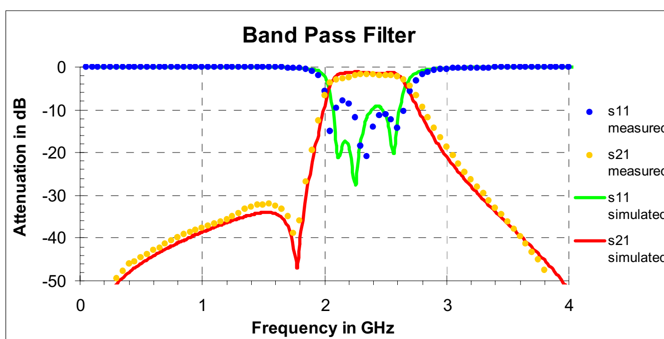


Figure 18: Simulated and measured attenuation for the band pass filter

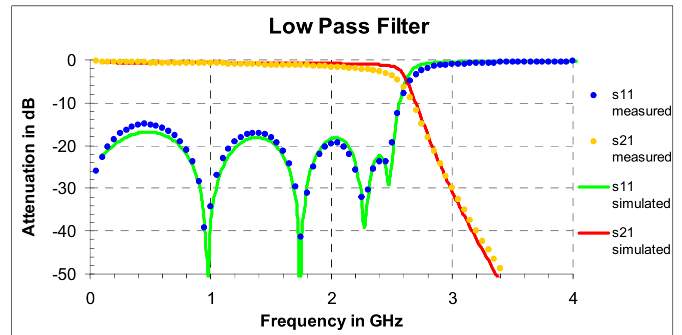


Figure 19: Simulated and measured attenuation for the low pass filter

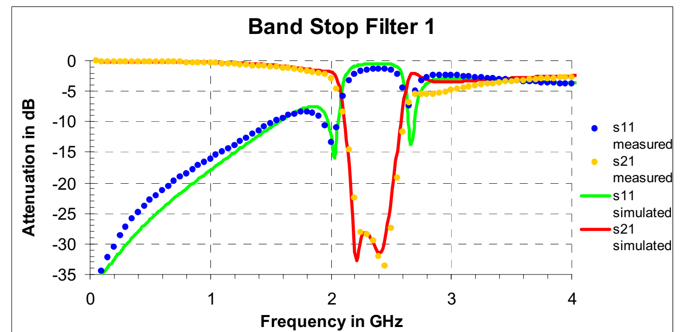


Figure 20: Simulated and measured attenuation for the band stop filter (6th order)

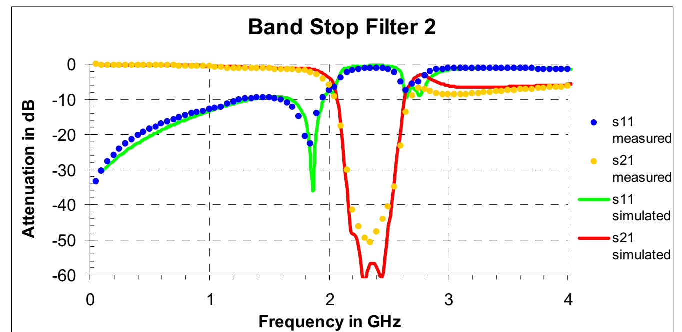


Figure 21: Simulated and measured attenuation for the band stop filter (10th order)

6. Flip chip mountable integrated passive device

The results regarding the integration of passives were used for the realization of an integrated passive device (IPD) to be used as input filter circuit for a Bluetooth chip [13].

One IPD contains three inductors of 3.9nH and 2 capacitors of 1.8fF realized in a copper BCB thin film build up on 4 inch glass substrates. A micro strip environment with 50Ω impedance was used to connect the elements to two low pass filters of second order and one single inductor within an area of 1.3mm by 2.6mm.

The IPD is designed as a flip chip device to be assembled as surface mountable component. Large solder balls with

500µm pitch were used as flip chip interconnects for SMT assembly, bringing the total component area to 2.6mm by 3.6mm.

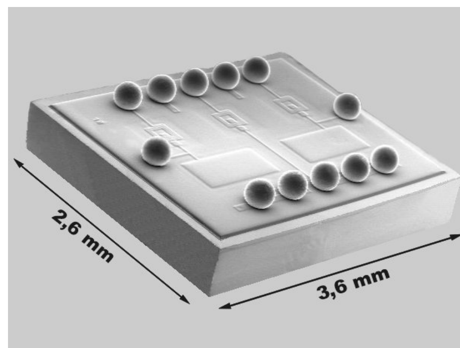
Compared to figure 1 the used thin film build up contains an additional BCB solder stop layer as well as an under bump metallization of copper, nickel and gold.

Figure 22 shows a secondary electron microscopy picture of an integrated passive device. Because of the BCB solder stop layer the components structures are blurred in this picture.

Figure 20 shows the measured attenuation of a low pass on an integrated passive device. Because of its low order the attenuation of this filter increases slower as for the low pass in figure 19.

Figure 22:

SEM picture of a flip chip mountable IPD



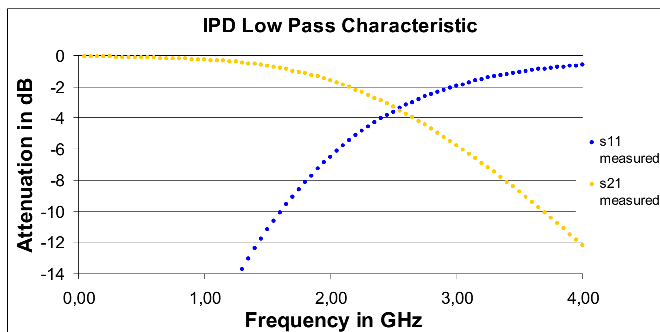


Figure 23: Measured attenuation for IPD low pass filter

7. Summary

Integrated passive components were successfully realized in a copper / BCB thin film build up using wafer level packaging technologies. Especially thin film coils in single and double layer fashion were examined regarding influences of their design parameters on their electrical behavior. Also passive filter structures for 2.4GHz were realized in the same build up. By using a design approach which considers the parasitic influences of the elements and conductors a good correspondence between simulation and measurement could be achieved. As a first application of the found results flip chip mountable integrated passive devices (IPDs) with integrated coils and capacitors were produced using wafer level fabrication.

The received results represent a solid base for the development of integrated passive structures to be used in future electronic products.

References

1. J. Dougherty, *"The NEMI Roadmap: Integrated Passives Technology and Economics"*, Proceedings of the Capacitor and Resistor Technology Symposium (CARTS), Scottsdale, AZ, April 2003
2. Prismark Partners LLC, *"Pushing the Shrinking Envelope – A Status Report on Embedded Passives in PWBs"*, December 2000
3. J. Dougherty, J. Galvangi, L. Marcanti, P. Sandborn, R. Charbonneau, R. Sheffield, *"The NEMI Roadmap Perspective on Integrated Passives"*, Proceedings of the European Microelectronics and Packaging Conference & Exhibition, Strasbourg, May 2001
4. H. Reichl, J. Wolf, *"Microelectronic Packaging – Ready for the Next Product Generation"*, HDI Conference, Santa Clara, April 17 – 20, 2001
5. M. Töpper, V. Glaw, R. Hahn, M. Schaldach, H. Reichl, *„Thin Film Multilayer Wiring with photosensitive BCB on Ceramic-, Thick Film- and LTCC-Substrates for MCMs (german)"*, SMT/ES&H/Hybrid '97, Nürnberg, April 22-24, 1997
6. V. Seidemann, S. Büttgenbach, *"An optimized fabrication process for microcoils utilizing UV-depth-lithography and BCB"*, Proceedings Vol. 1 Micro.Tec 2000, Hannover, September 25 – 27, 2000
7. M. Töpper, O. Ehrmann, H, Reichl, V. Glaw, J. Wolf, G. Fischbeck, K. Petermann, *„BCB – A Polymer for Thin Film Applications"*, MicroMat 1997, Berlin, April 16 – 18, 1997
8. K. Scherpinski, M. Töpper, F. Krause, K. Halser, R. Hahn, O. Ehrmann, H. Reichl, *„Integration of NiCr Resistors in a Multilayer Cu/BCB Wiring System"*, Int. Symp. and Exhibition on Advanced Packaging Materials, Braselton, USA, March 14 - 17 1999, pp. 178-185
9. Q. Tran, Q. Ma, *"High-Q, RF Inductors Fabricated Using WLP Redistribution Rechnology"*, IMAPS 2002, Denver, CO, Sept. 4-6
10. C.-W. Ju, S.-P. Lee, Y.-M. Lee, S.-B. Hyun, S.-S. Park, M.-K. Song, *„Embedded Passive Components in MCM-D for RF-Applications"*, Electronic Components and Technology Conference, Las Vegas, NV, May 21-24, 2000, pp. 211-214
11. D. Cottet, J. Grzyb, M. Scheffler, G. Tröster, *„Experimental Analysis of Design Options for Spiral Inductor Integrated on Low Cost MCM-D Substrates"*, Proc 51th Electronic Components and Technology Conf, Orlando, FL, May 29 - June 1, 2001, pp. 824-830
12. S. P. Morgan, *"Effect of Surface Roughness on Eddy Current Losses at Microwave Frequencies"*, Journal of Applied Physics, Volume 20, April 1949, pp. 352-362
13. T. Fritzsch, K. Zoschke, O. Ehrmann, J. Wolf, M. Töpper, K. Buschick, V. Glaw, H. Reichl, *„Modul for the Transmission of MPEG-4 Video Data using Bluetooth – Components and Packaging"*, Micro system technologies MST 2003, Munich, Okt. 7-8, 2003