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Properties of (In,Ga)(As,P)/GaAs interfaces grown under different metalorganic vapor phase epitaxy conditions

A. Knauer^{a,*}, P. Krispin^b, V.R. Balakrishnan^{b,1}, M. Weyers^a^a *Ferdinand-Braun-Institut für Höchstfrequenztechnik, Albert-Einstein-Str. 11, D-12489 Berlin, Germany*^b *Paul-Drude-Institut für Festkörperelektronik, Hausvogteiplatz 5-7, D-10117 Berlin, Germany*

Abstract

The mechanisms for formation of interlayers at the interface of GaAs on (In,Ga)P and $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}_{0.7}\text{P}_{0.3}$ grown by metalorganic vapor phase epitaxy have been studied by capacitance–voltage profiling of the electron concentration. Shallow In-rich quantum wells (QWs) are formed in (In,Ga)P during growth interruptions under PH_3 stabilization. These QWs are seen in C – V profiles, but not in photoluminescence and X-ray diffraction. Stabilization of (In,Ga)P under AsH_3 yields thin (1–2 nm thick) (In,Ga)(As,P) interlayers, which are observed by X-ray diffraction and capacitance–voltage profiles. Under optimized conditions, these interlayers exhibit negligibly small band offsets. When growing GaAs on quaternary (In,Ga)(As,P), interlayers can be avoided even at high growth temperatures and long growth interruptions. Independent on the chosen growth conditions, the (In,Ga)P and (In,Ga)(As,P) layers as well as the investigated interfaces are practically free of defect levels as determined by deep-level transient Fourier spectroscopy.

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1. Introduction

(In,Ga)(As,P) lattice matched to GaAs is an attractive alternative to the (Al,Ga)As/GaAs system for devices, because it is not affected by donor-related traps or the affinity of Al to oxygen. It is, however, well known from X-ray diffraction and mainly photoluminescence (PL) studies of

metalorganic vapor phase-epitaxy (MOVPE) grown GaAs/(In,Ga)P/GaAs structures that an interfacial layer may be formed on the $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$ layer (hereafter InGaP), which gives rise, in particular, to an additional low temperature PL peak around 1.4 eV [1–5]. Such layers strongly modify the electronic properties of the related heterointerface. Thus, often additional interlayers are deposited [1,2,5] and the gas switching/purging sequences [3] are optimized to avoid the occurrence of additional PL-peaks. But it is not clear yet, how this affects the electronic properties of lattice-matched (In,Ga)(As,P)/GaAs heterointerfaces grown by MOVPE. In the

*Corresponding author. Tel.: +49-30-6392-2673; fax: +49-30-6392-2685.

E-mail address: knauer@fbh-berlin.de (A. Knauer).

¹Permanent address: Solid State Physics Laboratory, Lucknow Road, Timarpur, Delhi 110054, India.

presence of sheet charges, capacitance–voltage ($C-V$) studies with metal–semiconductor contacts on isotype heterojunctions are known to provide reliable values for the band offset. We therefore use $C-V$ measurements to detect the inadvertent interlayers at the GaAs-on-(In,Ga)(As,P) interfaces by their conduction band offsets ΔE_C . Only in Refs. [5,6] in addition to the optical also the electrical characteristics of the InGaP/GaAs heterojunctions were investigated. The electronic properties of the normal [InGaP-on-GaAs] heterojunction are described in Ref. [6]. Therefore, our investigations focus on the compositional and electronic properties of GaAs on (In,Ga)(As,P) heterointerfaces grown by MOVPE under different conditions.

2. Experimental procedure

The investigated GaAs/InGaP/GaAs heterojunctions were grown in a horizontal MOVPE reactor (Aix 200) at 70 hPa on GaAs substrates using TMGa, TMIIn, Si₂H₆, PH₃, and AsH₃ as precursors. Nearly disordered InGaP alloys were grown at 580°C on (001)-oriented GaAs. Ordered InGaP layers [7] were realized at 650°C on singular (double-variant ordering) and vicinal (001) substrates with a miscut of 2° towards (1 $\bar{1}$ 1)B (single-variant ordering). V/III input ratios of 70 or 140 and growth rates of 2.5 μm/h were used. In_{0.15}Ga_{0.85}As_{0.70}P_{0.30} layers were deposited at 750°C on (001) GaAs with a growth rate of 1.4 μm/h and a V/III input ratio of 90. GaAs was grown with 1.2 μm/h at 580°C, 650°C or 750°C. V/III input ratios at 580°C and 650°C were 20, but 200 at temperatures higher than 700°C. The lattice mismatch of the layers determined by double-crystal X-ray diffraction was in all cases smaller than 5×10^{-4} . PL measurements were applied to verify the bandgap reduction due to long-range order [8]. In order to determine the electronic properties of the interfaces by the $C-V$ method (measurement frequency: 1 MHz), the layer structures were Si-doped with carrier concentrations in the 10^{17} cm^{-3} range (cf. Ref. [10]). Deep levels were investigated by deep-level transient Fourier spectroscopy (DLTFS) [9].

3. Results and discussion

For the deposition of GaAs on top of InGaP, the growth is interrupted for some time under PH₃ stabilization. To start the GaAs cap-layer deposition, the PH₃ is replaced by AsH₃. To study the impact of the stabilizing PH₃ flow on possible interfacial layer formation, the InGaP growth at 580°C and low V/III ratio was interrupted several times for 60 s under PH₃ stabilization. In the low temperature PL no additional anomalous peaks are observed. In the $C-V$ depth profile of the electron concentration n shown in Fig. 1, clear peaks are visible with depleted regions on both sides. This is characteristic for quantum wells (QWs). QWs with an In mole fraction larger than 0.49 are obviously formed as a result of the growth interruption. The fit of the measured electron distribution (see the line in Fig. 1) gives a well thickness of 20 nm and a conduction band offset of -2 meV (cf. Ref. [10]). The resulting carrier confinement (and In enrichment) in this very shallow QW is relatively small. Only a single PL peak is therefore observed for the InGaP/GaAs structure. Moreover, the corresponding lattice mismatch is too small to be seen in X-ray rocking curves. DLTFS measurements do not indicate any deep traps in connection with these shallow QWs. These results confirm the importance of In

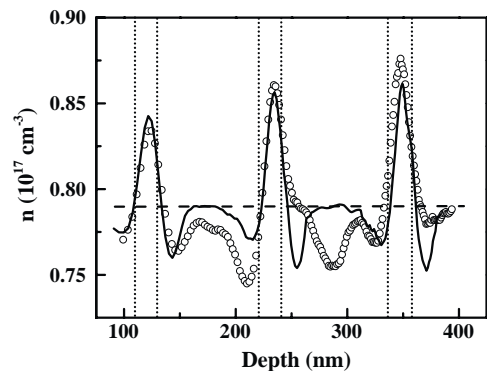


Fig. 1. Depth profile of the electron concentration n for an InGaP layer, deposited at 580°C with three growth interruptions of 60 s under PH₃ flux, measured at 80 K (circles). Solid line—simulated best fit, horizontal dashed line—doping level in InGaP, vertical dotted lines—marker for the interfaces of the interlayer.

carry-over for the formation of unintentional interfacial layers [2,3,11] even at low growth temperatures. Thus, long growth interruptions on InGaP surfaces should be avoided.

The growth of GaAs on InGaP is usually preceded by switching from PH_3 to AsH_3 and a stabilization of the surface under AsH_3 . When stabilizing the InGaP surface during the growth interruption at 580°C solely with AsH_3 for 60s, QWs are also formed. But, in contrast to the PH_3 stabilization, the compressive stress is so high, that the interlayers are clearly visible also in X-ray rocking curves. From X-ray simulation, their extension is found to be only 1–2 nm. It is therefore suggested, that As/P exchange plays a dominant role under AsH_3 , in contrast to the In carry-over effect and the subsequent incorporation of the excessive In in the interlayer formed under PH_3 . Again, the band offset of the QW is too small to get detected by low temperature PL measurements.

For the deposition of GaAs on InGaP, the growth was interrupted for about 5 s by switching off the TMGa- and TMin-flow. To start the GaAs deposition, PH_3 was directly replaced by AsH_3 , and 0.5 s later TMGa was switched on. For the nearly disordered InGaP layers grown at 580°C PL peak energies of 1.896 eV were measured at room temperature, while for the ordered InGaP grown at 650°C 1.842 eV was obtained for the double-variant and 1.815 eV for the single-variant order. In any case, the emission band at about 1.4 eV was missing suggesting sharp heterointerfaces for low V/III-ratios. The depth profiles of the electron concentration n for various GaAs-on-InGaP interfaces resulting from the more sensitive $C-V$ measurements are shown in Fig. 2. The profiles obviously strongly depend on the growth temperature, the V/III ratio, and the substrate orientation. While on (001) just oriented samples accumulation of carriers is seen on the GaAs side of the heterointerface, no such accumulation is observed for the miscut samples (curve 1). The apparent electron deficit can be minimized by growth at 580°C and high V/III ratio (curve 4). In contrast, a drastically enhanced carrier deficit at the interface is observed for single-variant ordered InGaP (curve 1). In order to check, whether the large

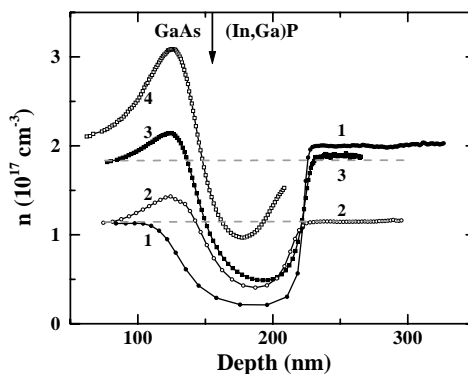


Fig. 2. Typical depth profiles of the carrier concentration n for GaAs-on-InGaP interfaces grown with a V/III ratio of 70 (1) at 650°C on a (001) substrate with 2° -off oriented to (1 $\bar{1}$ 1)B, (2) at 580°C and (3) at 650°C on exact (001) substrates. The sample of curve 4 was grown as (2), but with a doubled V/III ratio of 140. Dashed lines denote the constant doping levels for depth profiles 2 and 3.

carrier deficits at the GaAs-on-InGaP interface originate from deep interfacial levels, DLTFs measurements were performed (cf. Ref. [6]). On the InGaP side, electron traps are negligible. DLTFs responses, which could correspond to interfacial levels, are practically absent. The large carrier deficit at the interface is related to intrinsic electric fields as a result of the piezoelectric polarization of spontaneously ordered InGaP. The density of both interfacial charges increases with increasing degree of InGaP order [12]. $C-V$ measurements show that the used switching sequence and growth conditions avoid the formation of shallow QWs, which were observed for longer growth interruptions.

For a GaAs-on-InGaP interface, where the growth was interrupted for 360 s, in order to increase the growth temperature from 580°C to 750°C and the PH_3 flow from 75 to 300 sccm, the electron distribution is revealed in Fig. 3. Instead of the typical peak-valley structure for isotype heterojunctions, only carrier depletion on the InGaP side is seen at 300 K. At 80 K, an additional peak is observed at about 165 nm accompanied by a dip near 160 nm, corresponding to the intended depth of the GaAs-on-InGaP interface. Apparently, electrons are transferred from GaAs to an interlayer with a negative offset ΔE_{C2} . By

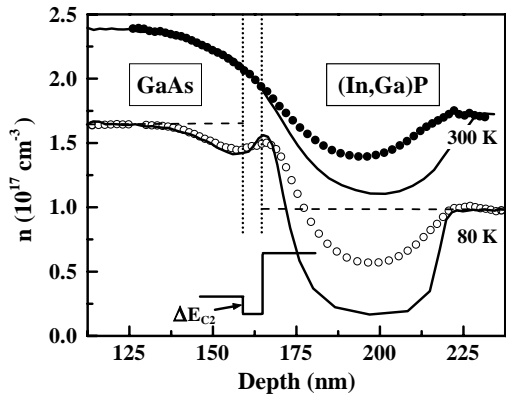


Fig. 3. Depth profiles of the electron concentration n for a GaAs-on-InGaP interface measured at 300 K (dots) and 80 K (circles). Elongation of growth interruption—360 s with temperature rise from 580°C to 750°C under increasing PH_3 flux from 75 to 300 sccm. The 300 K curve is vertically shifted for clarity. Full lines—simulated best fits, vertical dotted lines—marker for the interfaces of the interlayer, horizontal dashed lines—doping levels in GaAs and InGaP. Inset: conduction band diagram at the interface.

calculating the capacitance for an interface with the band diagram sketched in the inset of Fig. 3, the measured electron distributions can be well fitted on the GaAs side of the interface (see the lines in Fig. 3). The discrepancy on the InGaP side is associated with additional polarization charges, which are present inside the InGaP layer at the boundaries between ordered domains and the disordered InGaP matrix [10]. The fits in Fig. 3 result in a 6 nm thick interlayer with $\Delta E_{C2} = -0.012$ eV. This offset is due to compressively strained InGaP with an In mole fraction larger than 0.49 (cf. Fig. 1). The formation of such a compressively strained interlayer is confirmed by X-ray analysis. During the extended growth interruption under high PH_3 flow and at high temperature, In is apparently transported from the susceptor and is used to form the 6 nm thick compressively strained interlayer. In-rich layers are known to appear also at the surface of as-grown InGaP cooled down under PH_3 [13].

For comparison, GaAs was grown on quaternary $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}_{0.7}\text{P}_{0.3}$. Fig. 4 shows typical electron depth profiles of the electron concentration for two interfaces deposited under different

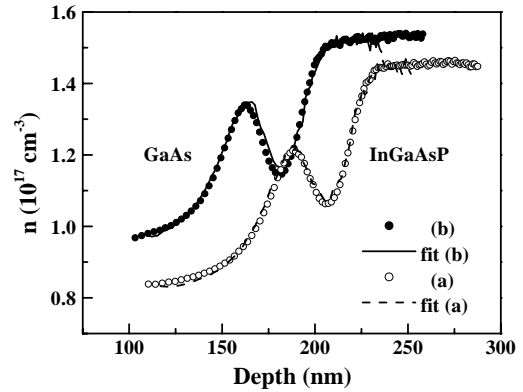


Fig. 4. Depth profiles of the electron concentration n for GaAs-on- $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}_{0.7}\text{P}_{0.3}$ interfaces grown (a) with 3 s growth interruption at 750°C (circles) and (b) with 600 s cooling down to 580°C under PH_3/AsH_3 flux (dots). Lines—simulated best fits.

growth conditions. In the first case (open circles in Fig. 4), the GaAs was deposited at 750°C after 3 s growth interruption (TMIn and TMGa flow off) by switching off PH_3 and switching on the TMGa flow again. In the second case (dots in Fig. 4), GaAs was deposited after 360 s cooling down from 750°C to 580°C. The typical clear accumulation of carriers on the GaAs side and the depletion on the $\text{In}_{0.15}\text{Ga}_{0.85}\text{As}_{0.7}\text{P}_{0.3}$ side are seen in both cases. The conduction band offset to GaAs is 46 meV. The curves can be well fitted by assuming abrupt heterointerfaces. In accordance with the $C-V$ measurements, unintentional interlayers could neither be detected by PL nor by X-ray measurements. Deep-level spectra of these structures do not show any defects at the interfaces or in the quaternary layers. The concentration of electron traps in the quaternary layers is estimated to be below $1 \times 10^{13} \text{ cm}^{-3}$. In addition, there are no extra sheet charges due to ordering. Lattice-matched quaternary (In,Ga)(As,P) layers with a relatively high arsenic content are apparently much more resistant to the formation of interlayers than InGaP. In contrast to the GaAs-on-InGaP interface, As/P-exchange and In carry-over have only negligible impact on the electrical and optical properties of GaAs-on-(In,Ga)(As,P) interfaces, even for longer interruptions at 750°C.

4. Conclusions

The C – V method is very sensitive to detect unintentional transition layers, which may be formed at the interface of GaAs-on-(In,Ga)(As,P) layer structures. It allows the optimization of epitaxial growth to minimize the formation of such interlayers, which often give rise to additional anomalous peaks in low-temperature PL spectra. By choosing growth conditions, which reduce the In carry-over as well as As/P-exchange during a growth interruption, the unintentional interlayers exhibit so small band offsets that they are not detected in low temperature PL and in most cases are of no practical importance for devices. Higher As and smaller In content in (In,Ga)(As,P) layers minimize the interlayer formation and allow much longer growth interruption and higher growth temperatures for stabilized surfaces. All the investigated interfaces were practically all defect free.

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