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# Fabrication and Electrical Performance of Oscillators in GaInP/GaAs-HBT MMIC Technology up to 40 GHz

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**Abstract.** The fabrication and electrical performance of monolithic coplanar 19- and 38-GHz oscillators in GaInP/GaAs-HBT MMIC technology are presented. Both fixed frequency and Voltage Controlled Oscillators (VCOs) have been realized. The fixed frequency oscillators show very low phase noise (PN), in case of the 19-GHz oscillator PN is -96 dBc/Hz, the 38-GHz oscillator reaches -89 dBc/Hz at 100 kHz offset.

## 1. Introduction

Low phase noise oscillators are one of the major building blocks both in sensor application and wireless communication systems. In order to reduce cost, monolithically integrated circuits (MMIC) are well suited. However, the active devices in MMICs have to show very low 1/f noise, because the quality factors of on-chip resonators are fairly low. Principally Heterojunction Bipolar Transistors (here: GaInP/GaAs-HBTs) show lower 1/f noise than Fieldeffect Transistors (e.g. AlGaAs/GaAs-HEMTs) because the current flow is perpendicular to semiconductor interfaces and thus the influence of interface and surface states on the output signal is drastically reduced.

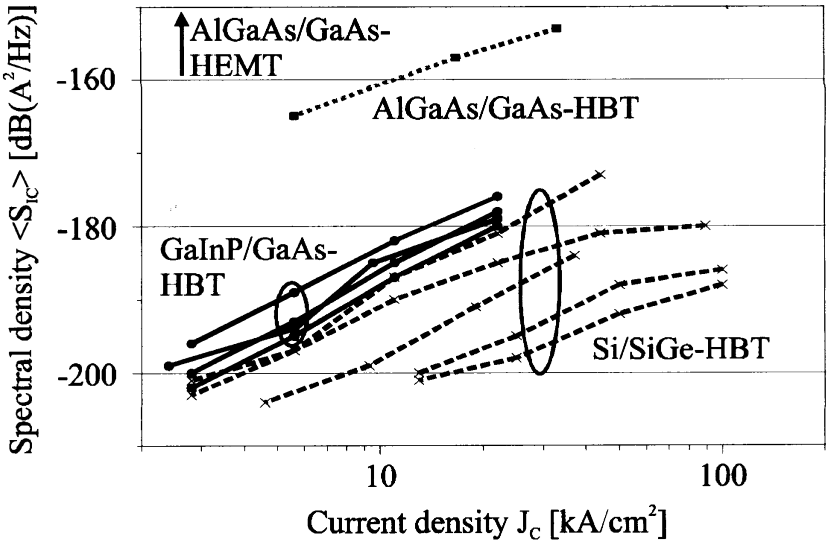

**Figure 1.** Measured 1/f noise levels of various devices vs. current density $J_C$ in dB($A^2$/Hz) at a frequency of 100 kHz (input resistance $R_S = 10\ \Omega$).

Although SiGe-HBTs demonstrate the lowest 1/f noise of all devices suitable for MMIC oscillators (see Fig. 1), these devices suffer from their frequency limitations and can hardly cover the emerging market for Ka- and W-band operation. GaInP/GaAs-HBTs fulfill both requirements and thus are well suited for low noise oscillators in the 20 - 77 GHz range.

## 2. Experimental

The epitaxial layer structures were grown by Metalorganic Vapor-Phase Epitaxy (MOVPE) on semi-insulating LEC-GaAs substrate. For the epitaxial HBT design a 55 nm $n^+$-InGaAs graded emitter-contact-layer, a 100 nm thick n-GaAs layer, a 30 nm n-InGaP emitter and a 100 nm uniformly doped p-GaAs base layer was used. Finally, the HBT structure was completed with a 1 µm n-GaAs collector, a 20 nm GaInP etch stop layer and a 700 nm thick $n^+$-GaAs subcollector.

The HBT MMICs were fabricated in-house using an industry-compatible 4" process line with stepper lithography [1]. In total 14 lithography levels were used.

From simulation experiments [2] two sources mainly affect the low frequency noise of HBTs: base current and 1/f noise of emitter resistance. In order to achieve low 1/f noise and high frequency levels especially the emitter-base-mesa fabrication is one of the most critical steps: With stronger under-etching of the emitter metal (used as etch mask) the distance from emitter to base-metalization increases. This leads to higher base-resistance $R_B$ and directly lower $f_{max}$. Similarly the cross-section area of the emitter decreases leading to a higher emitter resistance. Therefore a special double dry etch process has been developed combining anisotropic and isotropic etching. Since radiation damage strongly increases $R_B$ and causes surface recombination currents the anisotropic step must not reach the GaInP-emitter. Thus, in the first step 80 % of the InGaAs/GaAs emitter constact layer is etched anisotropic, in the second step the remaining GaAs is etched isotropic using the GaInP-emitter as etch stop layer (Fig. 2 a). To control the depth of each etch step an in situ interferometrical measuring unit (NanoMES®) was employed [3].

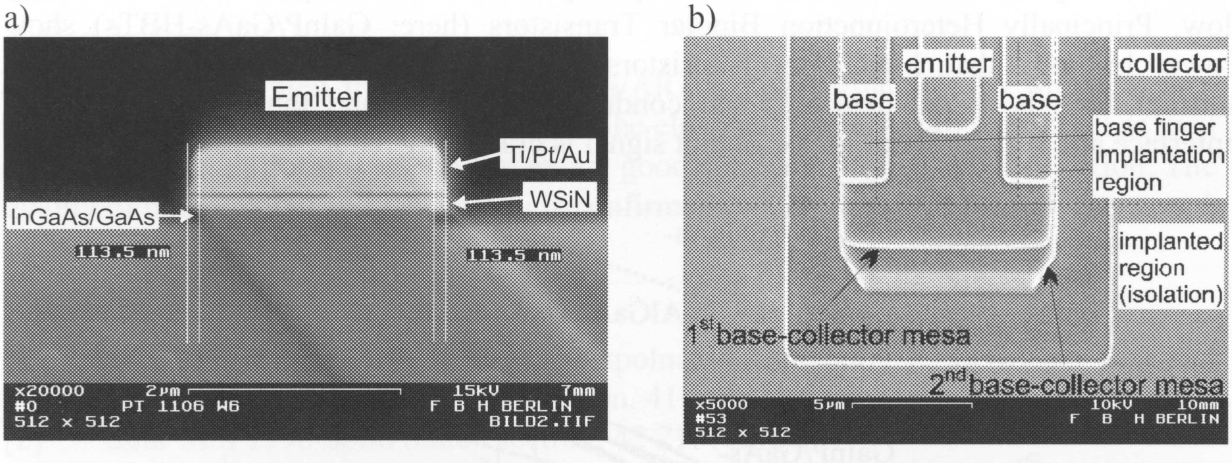

**Figure 2**. a) SEM cross section of the emitter area after emitter metalization and etching (typical: 90 - 120 nm); b) SEM photograph of an HBT after collector metalization.

Ledge technology was applied to suppress emitter-base-surface-leakage and further reduces 1/f noise. $He^+$-implantation was used for isolation between devices. Base-collector mesa was etched in two steps: in the first step dry etching was used to control the mesa width. In the second step wet chemical etching was applied in order to achieve under-etching and thus to reduce the parasitic base-collector capacitance $C_{BC}$ (see Fig. 2 b). An additional $He^+$-implantation in the outer region of the base fingers was introduced. In this way, the underlying base layer and the upper part of the collector (approx. 600 nm) are isolated and thus further reduction of $C_{BC}$ is achievable. For the

MMIC's passive elements MIM-capacitors (PECVD-$SiN_x$ as dielectric material), thin-film-resistors (sputtered NiCr), spiral-inductors, coplanar waveguides and air bridges (electroplated gold) were used.

## 3. Results

From process control monitoring (PCM) the gain $\beta_{max}$ is 120. With a corresponding intrinsic base sheet resistance $R_{SBI}$ of 215 Ω/sq the $\beta_{max}/R_{SBI}$-ratio is greater than 0.5 $(\Omega/sq)^{-1}$ indicating both excellent epitaxial material and device processing. Passive elements show very good uniformity over 4-inch wafer. In case of NiCr thin-film-resistivity the standard deviation $\sigma$ is 3.5 %. Using 110 nm thick $SiN_x$ for MIM-capacitors the breakdown voltage is around 70 V ( $E_{Br} > 6$ MV/cm, $\sigma < 2$ %) indicating the high quality PECVD-$SiN_x$. From S-parameter measurements $f_T$ and $f_{max}$ of our standard HBT (emitter-base-distance $d_{EB}$ = 1.3 μm, emitter area 1x3x30 $\mu m^2$) were determined to be 40 and 100 GHz, respectively. These values are quite sufficient for oscillators up to 40 GHz, but for future 77-GHz-oscillators $f_{max}$ has to be increased. Since

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}$$

drastic improvements can be achieved if the base resistance $R_B$ and the base-collector capacitance $C_{BC}$ are reduced. According to $R_B = R_{CB} + R_{SBE} * d_{EB}$ ($R_{CB}$: base contact resistance, $R_{SBE}$: extrinsic base sheet resistance) the base resistance drops down from 0.5 Ωmm to 0,25 Ωmm by reducing $d_{EB}$ from 1.3 to 0.5 μm. As can be seen from Fig. 3 in this way $f_{max}$ could be further increased to 150 GHz. By introduction of a shallow $He^+$-implantation in the outer region of the base fingers $C_{BC}$ could be further reduced leading to an $f_{max}$ of 170 GHz.

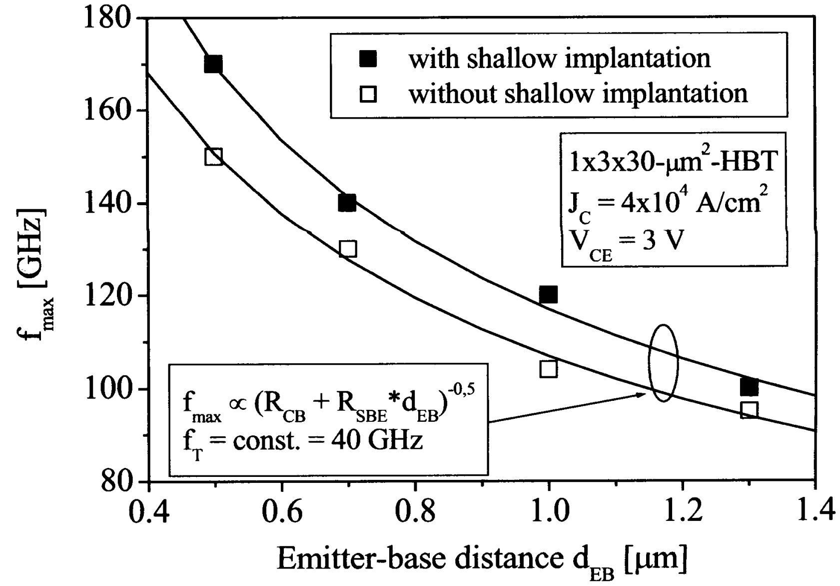

**Figure 3.** Maximum frequency of oscillation $f_{max}$ vs. emitter-base-separation $d_{EB}$ with and without shallow basefinger implantation.

As can be seen from Fig. 1 our HBTs show very low 1/f noise levels comparable to those of SiGe-HBT. It has to be mentioned that oscillators based on SiGe-HBTs typically run at higher current densities.

Fig. 4 illustrates our oscillator results. Details about oscillator simulations and measurement techniques were published in [4-6]. With single ended 19 GHz oscillator design the phase noise PN at 100 kHz offset exhibits very low levels and excellent uniformity over 4-inch ($\sigma < 2\%$, Fig. 4 a). Further improvements could be achieved with the push-push oscillator concept. Here we measured -96 dBc/Hz at the first harmonic of 19 GHz and -89 dBc/Hz at the second harmonic (Fig. 4 b). For the VCO version the PN is somewhat higher. Here the oscillator exhibits -86 dBc/Hz at the fundamental and -81 dBc/Hz at the second harmonic at 100 kHz offset.

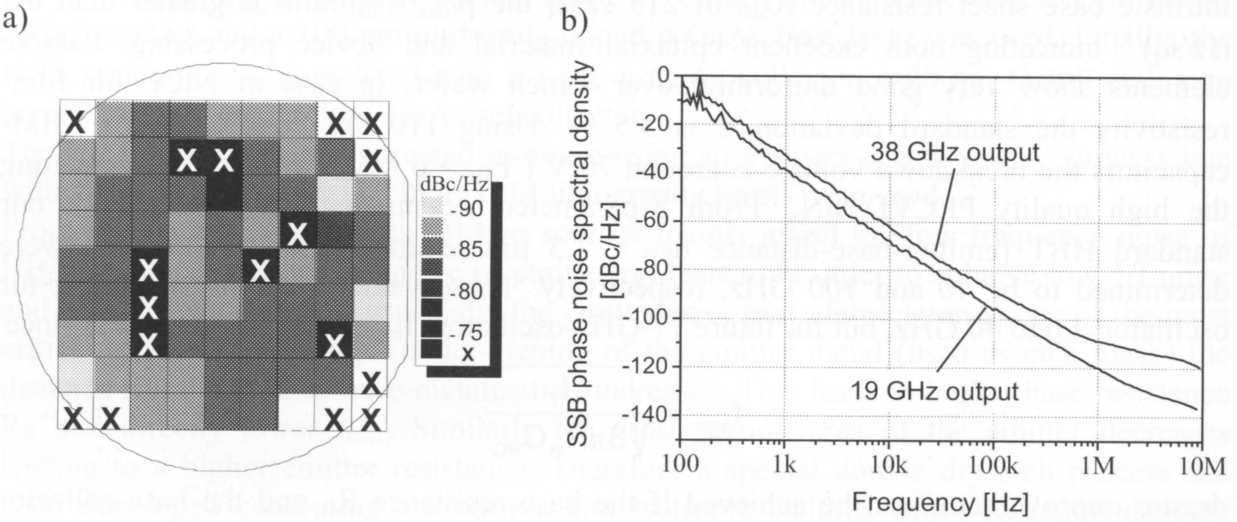

**Figure 4**. a) Phase noise map of a 19-GHz-oscillator (single ended, PN@ 100 kHz = -87.3± 1.7 dBc/Hz); b) phase noise of a 19-GHz differential oscillator (push-push design).

## 4. Summary

Fixed frequency oscillators and VCOs with low phase noise levels in the –90 dBc range were fabricated demonstrating the suitability of the GaInP/GaAs-HBT as the active device. By reducing parasitic elements of the HBT the maximum frequency of oscillation could be increased from 100 to170 GHz. Conclusively, these devices combine very good 1/f noise properties with the high frequency potential of GaAs-based transistors.

## 5. Acknowledgments

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