Mutual Interference in Calibration Line Configurations

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***Abstract* — When using multiline TRL calibrations for correcting on-wafer measurements, the accuracy of the result depends crucially on the consistency of the calibration set. For example, each line standard used in the calibration process must allow unambiguous measurements, i.e., the only difference between the various transmission-line elements should be line length. To this end, the pad structure for the probes, the probe mechanical contact properties and the environment including other structures, wafer or chip boundary and backside structures (metallization, chuck material) should be the same for each element. If this condition is not fulfilled, errors in the multiline TRL calibration process occur. This paper discusses the resulting deviations and presents some first rules for a proper layout of the calibration standards.**

***Index Terms* — Coupling, em simulation, measurements, parasitic modes, probes.**

I. Introduction

The multiline TRL (mTRL) calibration process is one of the most accurate 2-port calibration algorithms available for on-wafer measurements [1]. It is applicable in nearly any microstrip (MS) and coplanar waveguide (CPW) environment. It uses different line elements, e.g. lines of different lengths, a thru line, and an identical reflect on both ports (either short or open). These calibration elements are usually added on the wafer in the vicinity of the circuits to be characterized (DUTs). In order to save space the elements are usually positioned in a very dense configuration. Thus each element, especially those of the calibration set, may have different neighboring structures. The effect of these differences may be seen as small and, of course, the desired characteristics of the element will dominate the behavior of the measured parameters. But, the stray fields into the substrate from the probe at the contact pads will differ with the environment and thus influence field and wave excitation and propagation. These effects, though relatively small, will superimpose to the major characteristic and thus perturb the measurement result. For example, two completely identical calibration elements may lead to different measurement results when placed between different neighboring structures. This can happen for any line type standard, and most of the effects are similar in MS or CPW environment. But, depending on the line type, the effects are more or less strong. In this paper we will discuss the CPW case and study its electromagnetic behavior during probe measurement by experiment and simulation. The simulation was carried out using Microwave Studio from CST [2].

II. Investigated Setup and Line Elements

The investigated setup consists of a GaAs substrate with a dielectric constant of $\varepsilon_r = 12.9$ (Fig. 1) and a thickness of 500 µm placed on a ceramic chuck with a dielectric constant of $\varepsilon_r = 6$. In the electromagnetic simulation, a ceramic chuck thickness of 300 µm was used followed by an open boundary condition.

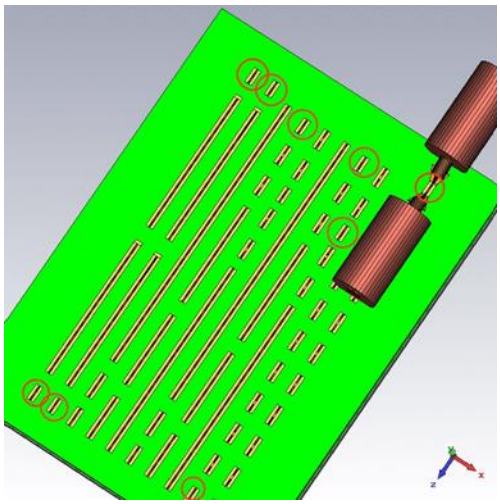

Fig. 1. The layout of the CPW calibration set with two probes positioned to contact a thru element (in this case: "align_4"). Further thru elements on the wafer are marked with circles.

The common parameters of the CPW lines are a signal width of 25 µm and 15 µm gap with 0.5 µm metal thickness using a conductivity of $\kappa = 3e7$ S/m, which yields about 50 ohms characteristic impedance.

As can be seen from Fig. 1, there is a large variety of lines available on this substrate, also containing lines with identical dimensions at different locations on the wafer. For instance, the thru element exists 10 times on the wafer, and the open element is available at 3 different locations.

III. Measurements, Simulation and Calibration

In the next step, the calibration set was measured and, at the same time, em-simulated. Then, the multiline TRL algorithm of [1] was applied to correct both the measurement and the simulation data. Therefore, a multiline TRL set on the GaAs wafer was defined, consisting of line elements 10000, 7115, 3700, 2685, 1600, 900 and 667 µm long, completed with an

additional thru element of 550 µm length. We choose the thru element "align_4" as the thru standard for multiline TRL. The reflect is represented by a 250 µm-offset short element. To allow a comparison against the simulation results, the measurement data was normalized to 50 ohms and the reference plane was shifted to the probe tips.

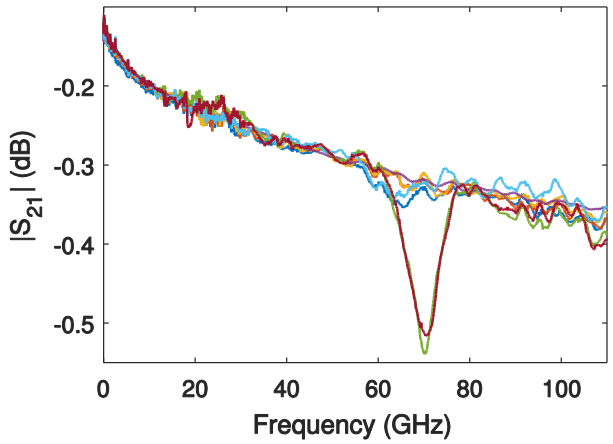

Fig. 2. Magnitude of measured S_{21} parameter of the supposed identical thru elements of the CPW calibration set. The multiline TRL calibration was performed with the thru element "align_4".

The measurements were performed with a semi-automated on-wafer prober system using an Anritsu VectorStar network analyzer in the frequency range from 0.1 to 110 GHz. For contacting the GaAs wafer structures, GGB Picoprobes 110H-GSG with 100 µm pitch were used. Measurements were taken on a ceramic chuck at constant temperature and relative humidity (23°C, 50% rel. H.).

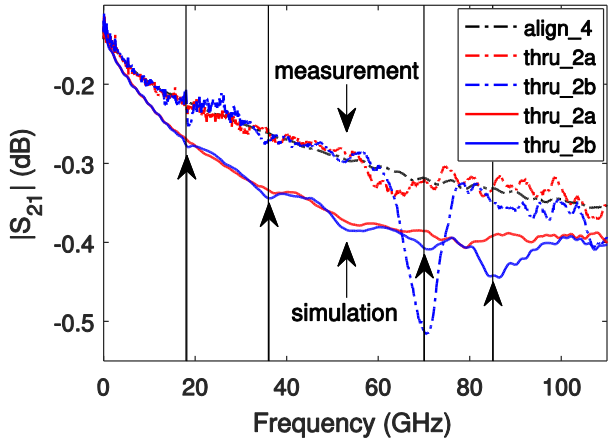

Fig. 3. Magnitude of measured S_{21} parameter of the thru elements "thru_2a" and "thru_2b" using line "align_4" as thru calibration device (dash-dotted line) compared to the CST simulations (solid line) of the same elements. Arrows indicate frequency points of field plots in Figs. 4–7.

Fig. 2 shows the magnitude of the corrected S_{21} measurement of all thru elements on the GaAs wafer. Since the thru elements all have the same dimensions, one does not expect deviations between the curves. The only differences between the elements are the structures in the neighborhood and the location on the wafer. Nonetheless, some of the thru elements show unexpected effects at certain frequencies.

To further investigate these effects, electromagnetic simulations of the thru elements with the most critical behavior were analyzed. In the following, we focus on the simulation results for the thru elements "thru_2a" and "thru_2b" (Fig. 3).

IV. Comparison of the Results

Fig. 3 shows the comparison of both measurement and simulation results of the multiline TRL corrected thru elements "thru_2a" and "thru_2b". Due to unknown design parameters of the probes and only limited knowledge of the material properties used in the measurement setup, a perfect overlap of measurement and simulation cannot be expected. However, the corresponding curves of both measurements and simulations show the same features at the frequencies where abnormal behavior occurs.

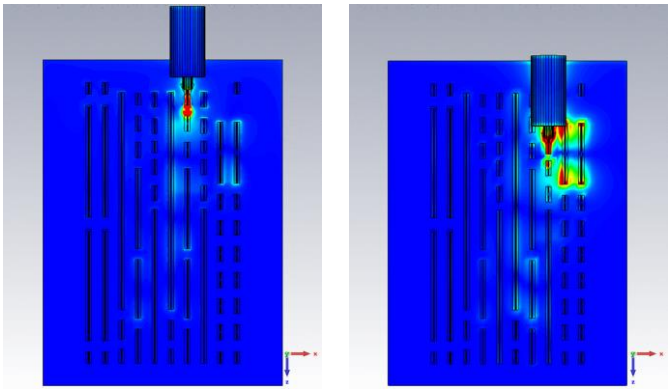

Fig. 4. Magnitude of electric field for the excitation of the "thru_2a" (left) and "thru_2b" (right) elements at 18 GHz.

Though the lines are physically and geometrically fully identical, noticeable deviations can be found. To identify the reasons for these deviations we studied the field and wave properties in the measurement set-up by simulation. Plots are taken for the specific frequencies marked in Fig. 3. Figs. 4–7 show the magnitude of the electrical fields at 18, 36, 70 and 85 GHz, respectively. Each figure shows the field plots for the excitation of "thru_2a" on the left-hand side and of "thru_2b" on the right-hand side. Only probe 2 of the two-port measurement setup is visible in all figures, probe 1 is hidden in order to not obstruct field observation. In general, we observe two pronounced effects. The first effect is that the fields are not at all confined to the intended structure but show significant spatial extension involving the neighboring line elements. In case of "thru_2a" the shown probe 2 and its tip opening is comparatively far away from any neighboring structures and partly outside of the wafer, while the same probe contacting "thru_2b" is surrounded in all directions by other line elements.

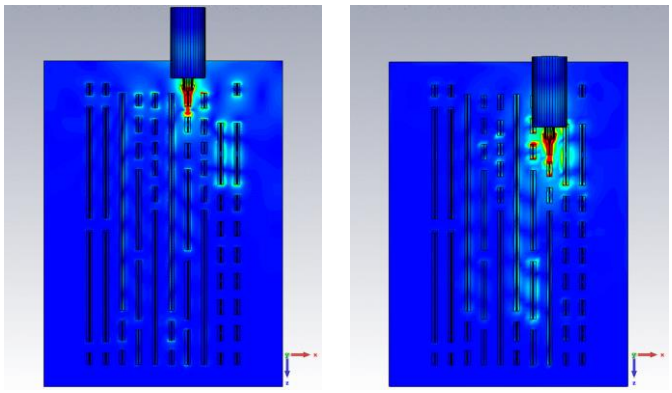

Fig. 5. Magnitude of electric field of Fig. 4 at 36 GHz.

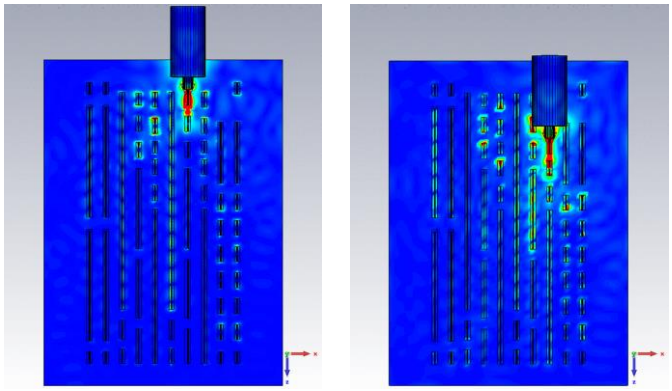

Fig. 6. Magnitude of electric field of Fig. 4 at 70 GHz.

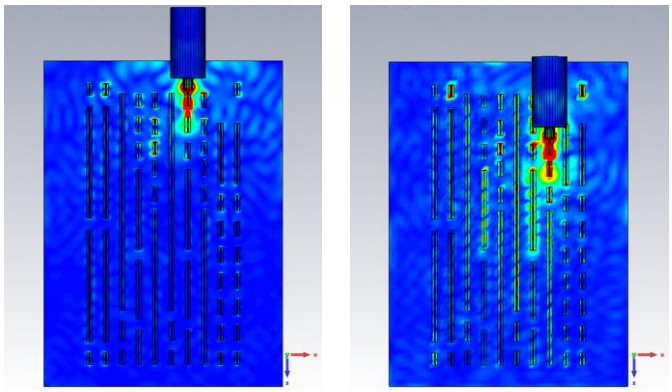

Fig. 7. Magnitude of electric field of Fig. 4 at 85 GHz.

The second effect is that the intensity of the stray fields increases with frequency and that more and more other elements become involved in the resulting behavior.

In the region around the probe tips and below the opening of the coaxial feeding line of the probe, fields are coupled into the substrate. Also, at the terminations of the measured CPW stray fields into the substrate are observed. Because there is no backside metallization, a parallel-plate mode does not exist and cannot be used for explanation. But different types of substrate modes can be excited and cause power leakage. In our case, we have two types of substrate modes. In regions outside CPW metallizations we have a 3-layer dielectric structure – ceramic chuck ($\varepsilon_r = 6$) – GaAs ($\varepsilon_r = 12.9$) – air. In regions with CPW metallization we have a two-layer dielectric – ceramic chuck ($\varepsilon_r = 6$) – GaAs ($\varepsilon_r = 12.9$) – CPW metallization. The electro-magnetic behavior of these modes is explained well in [3]–[6].

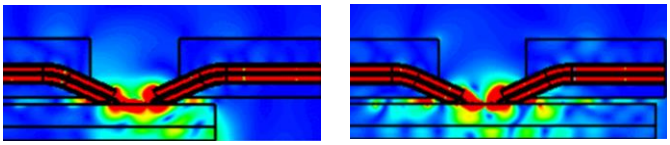

Fig. 8. Magnitude of electric field of the “thru_2a” (left) and “thru_2b” (right) elements in longitudinal direction at 85 GHz.

The propagation properties of these two modes differ but both modes propagate in the substrate. The 3-layer substrate mode is excited at the probe tips and spreads out into the substrate where it transforms into a 2-layer substrate mode at CPW metallizations continuing to travel under the CPW metallizations and there partly reflects and scatters back into the CPW modes. So, at the edges of the neighboring CPW the 3-layer substrate mode converts into a 2-layer substrate mode or is reflected. Thus, we see a very complex mixture of modes and waves in the wafer. Fig. 8 shows the fields and waves in the longitudinal cut of the thru elements at 85 GHz. The effect becomes rather strong. And again, due to the position on the wafer and due to the neighboring structures, the field and wave patterns in the substrate are different for the two geometries. The field plots in Fig. 9 add information on the transverse field pattern through the probe tips at 85 GHz.

Just to clarify the situation: One cannot avoid existence and excitation of substrate modes in such a dielectric layer system. However, one can minimize the feedback to the structure, i.e., reflection of substrate modes at the wafer boundary and the edges of the adjacent CPWs.

V. First Layout Rules

Obviously the neighborhood of a probed line element is important and cannot be neglected. In a CPW wafer environment using coaxial probes for measurement, the resulting effects can be separated into system-inherent problems, which cannot be solved without changing the probe and probe tip construction, and into effects which can be prevented by following some layout rules.

For higher frequencies where significant contributions by substrate modes are expected, it may be better not to use a layered dielectric substrate with different permittivities but only materials with similar dielectric constants. Thus the wave will radiate freely from the wafer into the chuck and fade away. This adds to the measurement error because power leakage occurs, but it describes the reality for DUTs in the same technology.

For the area around the probe one should consider at least twice the distance between probe tip and coaxial opening in longitudinal direction. In our example the length between

probe tip and coaxial opening length is appr. 400 µm and the distance between elements in the vicinity of the "thru_2b" is 350 µm only. The sideway pitch to the next element is 755 µm. Presently, it is difficult to specify a proper distance. From Figs. 4–7 one would suggest to double the pitch as shown there, i.e. appr. 1.5 mm.

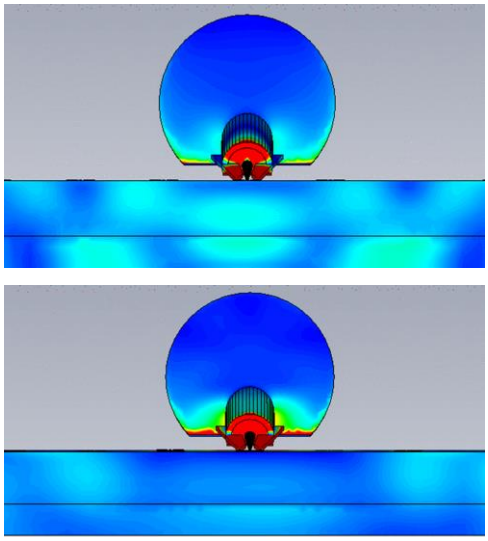

Fig. 9. Magnitude of electric field of the "thru_2a" (top) and "thru_2b" (bottom) elements in transversal direction through the probe tip at 85 GHz.

The given rules should be considered preliminary and are subject to further investigation. Simulation with a simplified probe model will show the regions around the probe tip where other structures should be avoided. For elements in close vicinity to the boundary the simulation will help to find appropriate distances. First simulations reveal an improvement for larger distances between DUTs (Fig. 10). At the present state of investigation a sideway and longitudinal distance of 1.6 mm (sideways layout distance 755 µm plus additional distance 800 µm) should be kept between elements. Due to the fact that the calibration set as shown in Fig. 1 was used, there are ripples created by the neighborhood of the calibration elements. Therefore the calibrated data of the DUT is still affected by the neighborhood effects of the calibration elements. Applying the additional distances also onto all calibration elements of Fig. 1 should result in a further improvement of the DUT correction which will be the next main focus of studies.

VI. Conclusions

Measuring CPW lines with coaxial microwave probes creates inevitably substrate modes and can give rise to further parasitic field effects. Using the measured results in calibration algorithms needs a proper survey of the calibration structures used. Measurement data of these structures can involve severe deviations due to parasitic effects by neighboring CPW elements, wafer boundaries or backside terminations. Some of these phenomena are inherent and cannot be avoided easily. Other effects, like coupling of substrate and other modes with neighboring lines or other discontinuities in the vicinity, can be avoided by following some simple design rules. The field investigations presented in this paper were used to develop some first design rules which at least help to reduce critical layout issues.

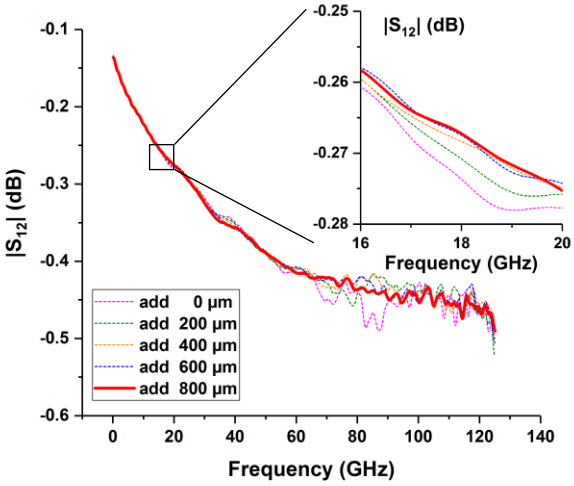

Fig. 10. Magnitude of simulated S_{12} of the "thru_2b"-line for different additional distances between the elements.

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